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DDR4
Odin MX 14N 16 N/V
& Antman 14/16

Alder Lake Schematic

2021-07
REV : X02

DY : None Installed
UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size: A4	Document Number: Odin ADL-P	Rev: SC
Date: Thursday, August 05, 2021	Sheet 1 of 105	

PCB PN : 203128-SC
Project Code
Odin14N : 4PD0Q9010001

Odin MX 14N 16 N/V & Antman 14/16 ADL-P Block Diagram

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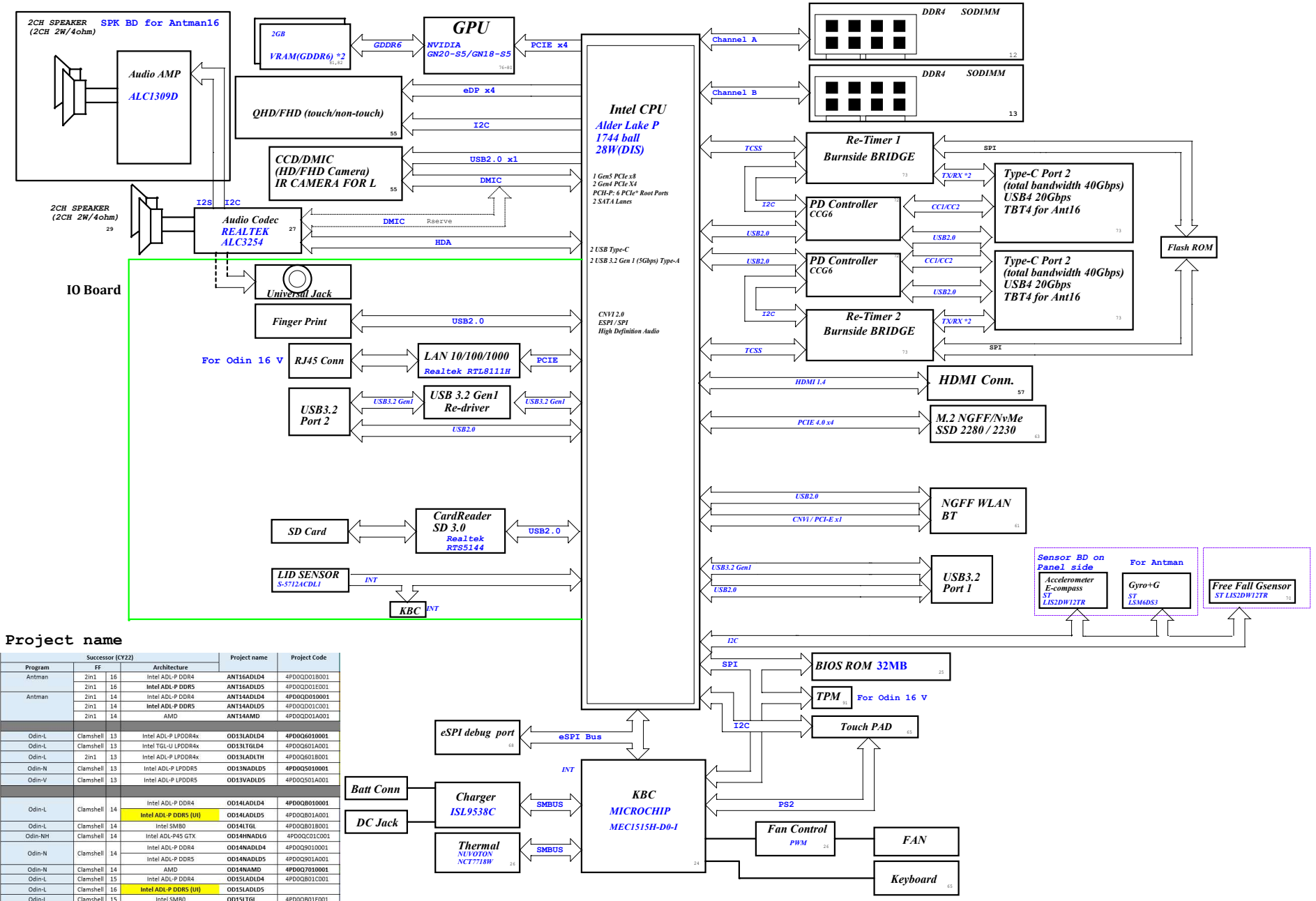

Project name

Successor (CY22)			Architecture	Project name	Project Code
Program	FF				
Antman	2in1	16	Intel ADL-P DDR4	ANT16ADLD4	4PD0QD01B001
	2in1	16	**Intel ADL-P DDR5**	ANT16ADLD5	4PD0QD01E001
Antman	2in1	14	Intel ADL-P DDR4	ANT14ADLD4	**4PD0QD010001**
	2in1	14	**Intel ADL-P DDR5**	ANT14ADLD5	4PD0QD01C001
	2in1	14	AMD	ANT14AMD	4PD0QD01A001
Odin-L	Clamshell	13	Intel ADL-P LPDDR4x	OD13LADLD4	**4PD0Q6010001**
Odin-L	Clamshell	13	Intel TGL-U LPDDR4x	OD13LTGLD4	4PD0Q601A001
Odin-L	2in1	13	Intel ADL-P LPDDR4x	OD13LADLTH	4PD0Q601B001
Odin-N	Clamshell	13	Intel ADL-P LPDDR5	OD13NADLD5	**4PD0Q5010001**
Odin-V	Clamshell	13	Intel ADL-P LPDDR5	OD13VADLD5	4PD0Q501A001
Odin-L	Clamshell	14	Intel ADL-P DDR4	OD14LADLD4	**4PD0QB010001**
			Intel ADL-P DDR5 (UI)	OD14LADLD5	4PD0QB01A001
Odin-L	Clamshell	14	Intel SM80	OD14LTGL	4PD0QB018001
Odin-NH	Clamshell	14	Intel ADL-P45 GTX	OD14HNADLG	4PD0QC01C001
Odin-N	Clamshell	14	Intel ADL-P DDR4	OD14NADLD4	4PD0Q9010001
			Intel ADL-P DDR5	OD14NADLD5	4PD0Q901A001
Odin-N	Clamshell	14	AMD	OD14NAMD	**4PD0Q7010001**
Odin-L	Clamshell	15	Intel ADL-P DDR4	OD15LADLD4	4PD0QB01C001
Odin-L	Clamshell	16	**Intel ADL-P DDR5 (UI)**	OD15LADLD5	
Odin-L	Clamshell	15	Intel SM80	OD15LTGL	4PD0QB01E001
Odin-L	Clamshell	14	AMD with AgS code	OD14LAMDAG	4PD0Q701C001
Odin-L	Clamshell	15	AMD with AgS code	OD15LAMDAG	4PD0Q701B001
Odin-N	Clamshell	16	Intel ADL-P28 DDR4	OD16NADLD4	4PD0Q901B001
			Intel ADL-P28 DDR5	OD16NADLD5	4PD0Q901C001
Odin-N	Clamshell	16	AMD	OD16NAMD	4PD0Q701E001
Odin-V	Clamshell	16	Intel ADL-P28 DDR4	OD16VADLD4	4PD0Q901F001
Odin-V	Clamshell	16	Intel ADL-P28 DDR5	OD16VADLD5	4PD0Q901E001
Odin-V	Clamshell	16	AMD	OD16VAMD	4PD0Q701A001
Odin-HN	Clamshell	16	Intel ADL-P45 GTX	OD16HNADLG	**4PD0QC010001**
Odin-HN	Clamshell	16	Intel ADL-P45 RTX	OD16HNADLR	4PD0QC01A001
Odin-VH	Clamshell	16	Intel ADL-P45 GTX	OD16HVADLG	4PD0QC01B001

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Title: Block Diagram
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Main Func = CPU

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22,24,44,46,72 PROCHOT_CPU_N
24 PECI_CPU

15 GPP_H0_BOOT_STRAP1
15 GPP_H1_BOOT_STRAP2
15 GPP_H2_BOOT_STRAP3

24,27 SPKR
15 DBG_PMODE

97 THERMTRIP_CPU_N

63 M2_PCIE_LED#
24,64 MASK_SATA_LED#
24 NB_MODE#
24,64 BATT_WHITE_LED#
55 W_INT

55 TOUCH_PANEL_DETECT#

24,66 LID_CL_SIO_TAB#

24 SAR_SENSOR_INT#

5.6.6.1 THERMTRIP

5.6.6.1.1 THERMTRIP Topology

Pcb Type: None

Pcb Thickness: None

Figure 155. CPU Sideband - THERMTRIP

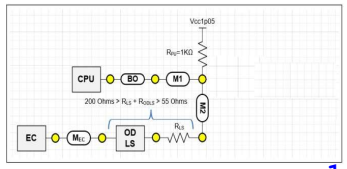

Table 337. THERMTRIP Topology Notes

Note	Detail
Platform resistors values	Rpu=1KΩ, Rls+Rodls=55-200Ω
Platform resistors tolerances	0.05
EC connection	Connection to EC is optional. EC could also be another monitoring agent.

Segment Lengths

Max Length Total (mm): 510

DMI	DMI_RCOMP	50ohm±1% pull-down to GND	0.8	-	
CPU MISC	PROC_POPIRCOMP	50ohm±1% pull-down to GND	0.8	-	

PROCHOT_CPU_N R310 1 2 499R2F-2-GP

R313 2 1 49D9R2F-L1-GP PROC_RCOMP
R314 2 1 49D9R2F-L1-GP DMI_RCOMP

1.8V LID_CL_SIO_TAB#

1.8V ISH_NB_MODE

R315 2 1 100KR2J-1-GP LID_CL_SIO_TAB#
ISH_NB_MODE
TP306 1 TOUCH_PANEL_DETECT#

CPU1V

CPU_CATERR_N	AF15	CATERR#	
PECI_CPU	DG3	PECI	
PROCHOT_CPU_N	AK32	PROCHOT#	
THERMTRIP#_CPU_N	AH32	THERMTRIP#	
PROC_RCOMP	DV60	PROC_POPIRCOMP	
DMI_RCOMP	DG1	DMI_RCOMP	
	DV11	TP#DV11	
	DV10	TP#DV10	
DBG_PMODE	ET14	DBG_PMODE	
LID_CL_SIO_TAB#	EB56	GPP_B4/PROC_GP3/ISH_GP5B	
ISH_NB_MODE	EB57	GPP_B3/PROC_GP2/ISH_GP4B	
TOUCH_PANEL_DETECT#	EY23	GPP_E7/PROC_GP1	
		GPP_E3/PROC_GP0	
GPP_H2_BOOT_STRAP3	ET46	GPP_H2	
GPP_H1_BOOT_STRAP2	EL48	GPP_H1	
GPP_H0_BOOT_STRAP1	EK48	GPP_H0	
SAR_SENSOR_INT#	DY61	GPP_B15/TIME_SYNC0/ISH_GP7	
SPKR	DW56	GPP_B14/SPKR/TIME_SYNC1/SATA_LED#/ISH_GP6	

PROC_JTAG_TRST#	R6	CPU_JTAG_TRST_N	
PROC_JTAG_TMS	U8	CPU_JTAG_TMS	
PROC_JTAG_TDO	AA6	CPU_JTAG_TDO	
PROC_JTAG_TDI	W8	CPU_JTAG_TDI	
PROC_JTAG_TCK	N6	CPU_JTAG_TCK	
PCH_JTAGX	N8		
PCH_JTAG_TMS	U6		
PCH_JTAG_TDO	AA8		
PCH_JTAG_TDI	W6		
PCH_JTAG_TCK	FB6	PCH_JTAG_TCK	
PCH_PROC_TRST#	R8		
PROC_PREQ#	L6	CPU_JTAG_PREQ_N	1 TP304
PROC_PRDY#	L8	CPU_JTAG_PRDY_N	1 TP305
EAR#	AF25	CPU_EAR_N	
GPP_F7	EN28		
GPP_F9/BOOTMPC	ET28	GPP_F7	
GPP_F10	EF28	GPP_F10 STRAP PIN DON'T USE	

ALDER-LAKE-P-GP-U1

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Q301

1		6	NB_MODE#
ISH_NB_MODE	2	5	MASK_SATA_LED#
BATT_WHITE_LED#	3	4	M2_PCIE_LED#

3rd = 075.00138.0F7C
2nd = 075.00139.007C
075.00138.0A7C
PJT138KA-GP

1D8V_S5

R318 10KR2J-3-GP

NB_MODE#

1D8V_S0

R317 ANT16 2 10KR1J-GP W_INT

1D05V_VCCST

R311 1 1KR2J-1-GP CPU_CATERR_N
R316 1 1KR2J-1-GP PROCHOT_CPU_N
R312 1 2 1KR2F-3-GP THERMTRIP_CPU_N

Put these resistor to close PCH side

R305 1 XDP 2 51R2J-2-GP CPU_JTAG_TDI
R306 1 XDP 2 51R2J-2-GP CPU_JTAG_TMS

R303 1 100R2J-2-GP CPU_JTAG_TDO

CAD NOTE:

Place strapping resistor within 6.35mm of main hook[2] to cfg[0] trace.

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm

1D05V_VCCST

R301 1 1KR1F-GP CPU_EAR_N

According to MOW-WW50, The EAR pin Pull-Up is updated to VCC1P05_PROC 2020/12/14

CAD NOTE:

Place within 27.94mm of CPU JATG TCK pin in Layout

R309 2 DY 1 51R2J-2-GP PCH_JTAG_TCK
R304 2 1 51R2J-2-GP CPU_JTAG_TCK

Table 809. Debug Port Signal Mapping

MIPI60 Pin#	Intel DPS Generic Signal name	Target System Signal Name	Direction from tool	Device	Components	Notes
3	TCK0	CPU_JTAG_TCK		CPU	51Ω to GND	Add CAD note to place within 27.94mm of CPU_JTAG_TCK pin in Layout
		PCH_JTAGx		PCH	N/A	Internal 60Ω - 100Ω ODT to GND in PCH.
51	TCK1	PCH_JTAG_TCK		PCH	**empty** 51Ω to GND resistor	Defensive, A0 PO boards only. Internal 60Ω - 100Ω ODT to GND in PCH. Add CAD note to place within 27.94mm of PCH_JTAG_TCK pin in Layout
9	TRST_N	CPU_JTAG_TRST_N		CPU	N/A	Internal 50Ω ODT to GND in PCH.
		PCH_CPU_JTAG_TRST_B		PCH	N/A	
2	TMS	CPU_JTAG_TMS		CPU	N/A	Internal 50Ω ODT to VccSTG in CPU
		PCH_JTAG_TMS		PCH	51Ω to VccSTG_OUT_LGC	
5	TDI	CPU_JTAG_TDI		CPU	N/A	Internal 50Ω ODT to VccSTG in CPU
		PCH_JTAG_TDI		PCH	51Ω to VccSTG_OUT_LGC	

continued...

<Core Design>

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Title: 003_CPU (PEG/DMI/PCIE4.0)

Size: A3 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 3 of 105

Main Func = CPU

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eDP

55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU
55 eDP_VDD_EN
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU

HDMI

57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_DET_CPU

Type-C #2 (TBT4)

75 USB2_TCSS_TX_N0
75 USB2_TCSS_TX_P0
75 USB2_TCSS_TX_N1
75 USB2_TCSS_TX_P1
75 USB2_TCSS_RX_N0
75 USB2_TCSS_RX_P0
75 USB2_TCSS_RX_N1
75 USB2_TCSS_RX_P1
75 USB2_TCSS_AUX_N
75 USB2_TCSS_AUX_P
75 USB2_TCSS_TXD
15,75 USB2_TCSS_RXD

Type-C #1 (TBT4)

71 USB1_TCSS_TX_N0
71 USB1_TCSS_TX_P0
71 USB1_TCSS_TX_N1
71 USB1_TCSS_TX_P1
71 USB1_TCSS_RX_N0
71 USB1_TCSS_RX_P0
71 USB1_TCSS_RX_N1
71 USB1_TCSS_RX_P1
71 USB1_TCSS_AUX_N
71 USB1_TCSS_AUX_P
15,71 USB1_TCSS_RXD

STRAP

15 USB3_TCSS_RXD
15 USB4_TCSS_RXD

71 USB1_TCSS_TXD
72 PD1_SOC_OC_FAULT_R
72 PD2_SOC_OC_FAULT_R

61 WIFI_RF_EN
55 TOUCH_PANEL_RST#_R
61 WLAN_WAKE_N
65 KB_DET#
55 CAMERA_2ND_DET

CPU1A — 1 OF 22

eDP

eDP_TX_CPU_P3 W3 — DDIA_TXP3
eDP_TX_CPU_N3 AA3 — DDIA_TXN3
eDP_TX_CPU_P2 AA1 — DDIA_TXP2
eDP_TX_CPU_N2 AB1 — DDIA_TXN2
eDP_TX_CPU_P1 AB3 — DDIA_TXP1
eDP_TX_CPU_N1 AD3 — DDIA_TXN1
eDP_TX_CPU_P0 AF1 — DDIA_TXP0
eDP_TX_CPU_N0 AD1 — DDIA_TXN0
eDP_AUX_CPU_P AF3 — DDIA_AUXP
eDP_AUX_CPU_N AG3 — DDIA_AUXN

GPP_E22 STRAP PIN DON'T USE

CAMERA_2ND_DET ER23 / ET23 — GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA

eDP

eDP_HPD_CPU EV25 — GPP_E14/DDSP_HPDA/DISP_MISC_A

HDMI

HDMI_DDI_TX_P3 AP6 — DDIB_TXP3
HDMI_DDI_TX_N3 AP8 — DDIB_TXN3
HDMI_DDI_TX_P0 AM6 — DDIB_TXP2
HDMI_DDI_TX_N0 AM8 — DDIB_TXN2
HDMI_DDI_TX_P1 AK6 — DDIB_TXP1
HDMI_DDI_TX_N1 AK8 — DDIB_TXN1
HDMI_DDI_TX_P2 AH6 — DDIB_TXP0
HDMI_DDI_TX_N2 AH8 — DDIB_TXN0
AE6 — DDIB_AUXP
AE8 — DDIB_AUXN

HDMI

HDMI_SCL_CPU EK46 — GPP_H15/DDPB_CTRLCLK/PCIE_LINK_DOWN
HDMI_SDA_CPU EL46 — GPP_H17/DDPB_CTRLDATA
HDMI_DET_CPU EB47 — GPP_A18/DDSP_HPDB/DISP_MISCB

WIFI_RF_EN DV54 — GPP_A21/DDPC_CTRLCLK
KB_DET# DV52 — GPP_A22/DDPC_CTRLDATA

Type-C #1

USB1_TCSS_TXD ER26
USB1_TCSS_RXD ET26 — GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD/BSSB_LS0_RX
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD/BSSB_LS0_TX

Type-C #2

USB2_TCSS_TXD EL26
USB2_TCSS_RXD EN26 — GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD/BSSB_LS1_RX
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD/BSSB_LS1_TX

USB3_TCSS_RXD FC37 / EV37 — GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/BSSB_LS2_RX/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/BSSB_LS2_TX/GSPI2_CLK

USB4_TCSS_RXD EY37 / FA37 — GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/BSSB_LS3_RX/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/BSSB_LS3_TX/GSPI2_MOSI

TOUCH_PANEL_RST#_R DY54 — GPP_A17/DISP_MISCC
WLAN_WAKE_N EB49 — GPP_A19/DDSP_HPD1/DISP_MISC1
EB51 — GPP_A20/DDSP_HPD2/DISP_MISC2

PD2_SOC_OC_FAULT_R DY47 — GPP_A14/USB_OC1#/DDSP_HPD3/DISP_MISC3
PD1_SOC_OC_FAULT_R DY49 — GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4

eDP

eDP_VDD_EN ET21 — VDDEN
eDP_BLEN_CPU EN21 — EDP_BKLTEN
eDP_BLCTRL_CPU EL21 — EDP_BKLTCTL

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Type-C (USB1)

TCP0_TXRX_P1 BE8 — USB1_TCSS_RX_P1
TCP0_TXRX_N1 BE6 — USB1_TCSS_RX_N1
TCP0_TXRX_P0 BG8 — USB1_TCSS_RX_P0
TCP0_TXRX_N0 BG6 — USB1_TCSS_RX_N0
TCP0_TX_P1 AY3 — USB1_TCSS_TX_P1
TCP0_TX_N1 BB3 — USB1_TCSS_TX_N1
TCP0_TX_P0 BD3 — USB1_TCSS_TX_P0
TCP0_TX_N0 BE3 — USB1_TCSS_TX_N0
TCP0_AUX_P BB1 — USB1_TCSS_AUX_P
TCP0_AUX_N BD1 — USB1_TCSS_AUX_N

Type-C (USB2)

TCP1_TXRX_P1 AV8 — USB2_TCSS_RX_P1
TCP1_TXRX_N1 AV6 — USB2_TCSS_RX_N1
TCP1_TXRX_P0 AY8 — USB2_TCSS_RX_P0
TCP1_TXRX_N0 AY6 — USB2_TCSS_RX_N0
TCP1_TX_P1 AP3 — USB2_TCSS_TX_P1
TCP1_TX_N1 AR3 — USB2_TCSS_TX_N1
TCP1_TX_P0 AU3 — USB2_TCSS_TX_P0
TCP1_TX_N0 AW3 — USB2_TCSS_TX_N0
TCP1_AUX_P AR1 — USB2_TCSS_AUX_P
TCP1_AUX_N AU1 — USB2_TCSS_AUX_N

TCP2_TXRX_P1 BN8
TCP2_TXRX_N1 BN6
TCP2_TXRX_P0 BL8
TCP2_TXRX_N0 BL6
TCP2_TX_P1 BK3
TCP2_TX_N1 BM3
TCP2_TX_P0 BG3
TCP2_TX_N0 BH3
TCP2_AUX_P BH1
TCP2_AUX_N BK1

TCP3_TXRX_P1 BW8
TCP3_TXRX_N1 BW6
TCP3_TXRX_P0 BU8
TCP3_TXRX_N0 BU6
TCP3_TX_P1 BU3
TCP3_TX_N1 BV3
TCP3_TX_P0 BN3
TCP3_TX_N0 BR3
TCP3_AUX_P BR1
TCP3_AUX_N BU1

VSS AL3
TCP_RCOMP AM1 — TCSS_RCOMP — R404 2 1 2K2R2F-GP

DISP_UTILS_2 AF32

DDIA_RCOMP AJ1 — eDP_RCOMP — R401 2 1 150R2F-1-GP
DDIB_RCOMP AL1 — eDP2_RCOMP — R402 2 1 150R2F-1-GP

DISP_UTILS_1 DJ1

DESIGN NOTE:
Stuff R404 with 2.2K for ADL P silicon

CAD NOTE:
TCRCOMP Resistor place as near as possible to SOC pins

3D3V_S0
R405 1100KR1J-GP KB_DET#

Table 165. TCP Port Signal Mapping For DisplayPort*

Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3

Note: Apply to TCP ports only.

3.7 RCOMP

The RCOMP recommendation for various interfaces provided below:

Table 29. RCOMP Recommendation

Interface	Pin Name	Board Rterm (Ohm)	Board DC resistance (ohms)	Board parasitic capacitance (pF)	Notes
Type C	TCP_RCOMP	2.2k +/- 1% to GND	<0.015	1.4	
Display	DDIB_RCOMP	150 ohm +/-1% pull-down to GND	<0.2	-	No Cself requirement. Rdc <0.5 ohm PKG + Board
Display	DDIA_RCOMP	150 ohm +/-1% pull-down to GND	<0.15	-	No Cself requirement. Rdc <0.5 ohm PKG + Board

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 004_CPU (DDI/EDP/TCP/DP/CSI)
Size: Custom | Document Number: Odin ADL-P | Rev: SC
Date: Thursday, August 05, 2021 | Sheet 4 of 105

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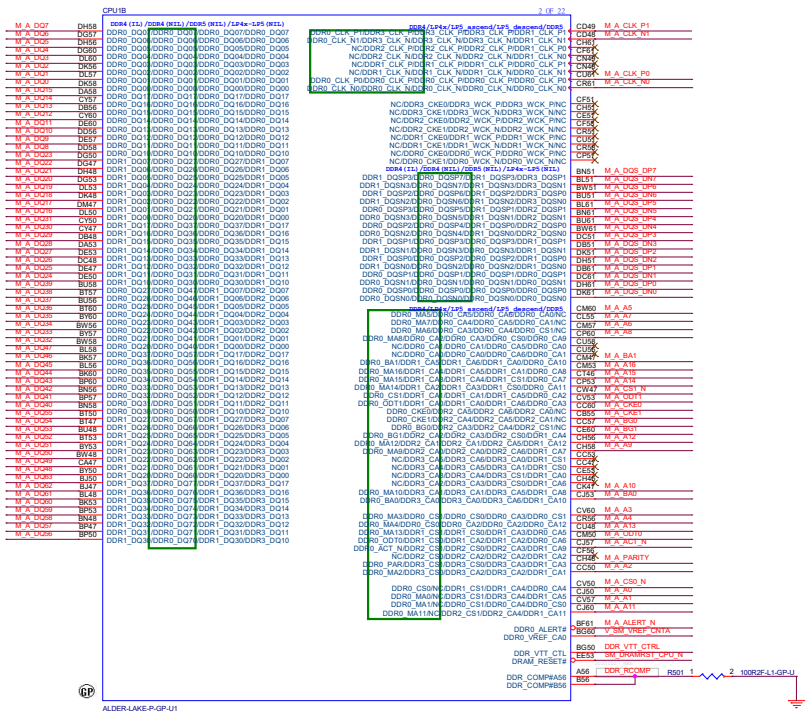
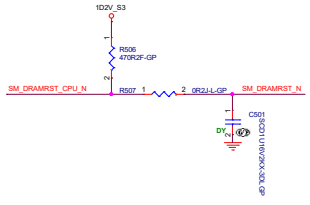
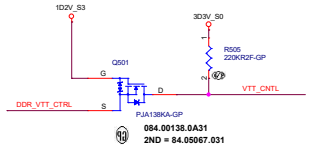
Non-Interleaved Type







084.00138.0A31
2ND = 84.05067.031

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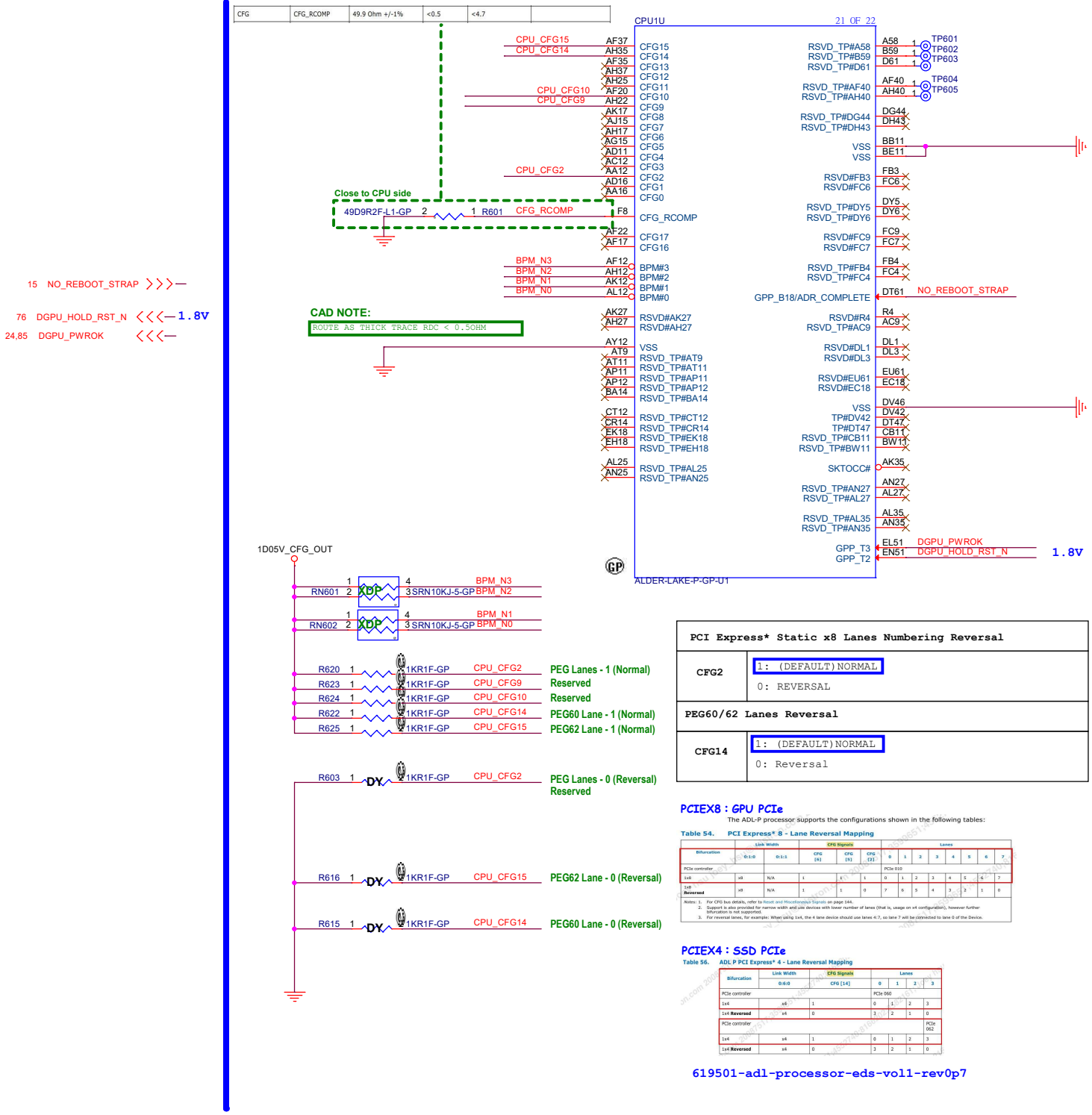
Taipei Hsien 221, Taiwan, R.O.C.

Title: 005_CPU (DDR)

Size	Document Number	Rev
Custom	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 5 of 105

Main Func = CPU



PCI Express* Static x8 Lanes Numbering Reversal	
CFG2	1: (DEFAULT) NORMAL 0: REVERSAL
PEG60/62 Lanes Reversal	
CFG14	1: (DEFAULT) NORMAL 0: Reversal

PCIEX8 : GPU PCIe

The ADL-P processor supports the configurations shown in the following tables:

Table 54. PCI Express* 8 - Lane Reversal Mapping

Bifurcation	Link Width	CFG Signals			Lanes							
	0:1:0	0:1:1	CFG [4]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7
PCIe controller			PCIe 010										
1x8	x8	N/A	1	1	1	0	1	2	3	4	5	6	7
1x8 Reversed	x8	N/A	1	1	0	7	6	5	4	3	2	1	0

Notes: 1. For CFG bus details, refer to Reset and Miscellaneous Signals on page 144.
2. Support is also provided for narrow width and uxie devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. For reversal lanes, for example: When using 1x4, the 4 lane device should use lanes 4:7, so lane 7 will be connected to lane 0 of the Device.

PCIEX4 : SSD PCIe

Table 56. ADL P PCI Express* 4 - Lane Reversal Mapping

Bifurcation	Link Width	CFG Signals	Lanes			
	0:0:0	CFG [14]	0	1	2	3
PCIe controller			PCIe 060			
1x4	x4	1	0	1	2	3
1x4 Reversed	x4	0	3	2	1	0
PCIe controller			PCIe 062			
1x4	x4	1	0	1	2	3
1x4 Reversed	x4	0	3	2	1	0

619501-adl-processor-eds-vol1-rev0p7

5.7 CFG Signals Functionality and Termination

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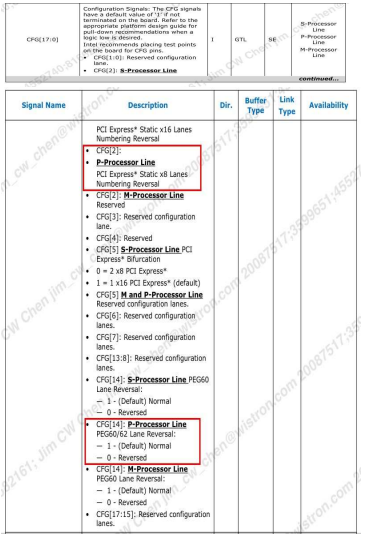
Table 349. CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	none	
CFG[2]	PCI Express* Static X8 Lane Numbering Reversal • 1:Normal Operation • 0: Lane Numbers reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[5]	RSVD	None	
CFG[6]	RSVD	NONE	
CFG[8:7]	RSVD	None	
CFG[10:9]	RSVD	Pull -Up to VCC_CFG_PU_OUT	1K Ohm
CFG[13:11]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull-up to VCC_CFG_PU_OUT/ / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

627205_ADL P_PDG_SchChk_Rev0p81

11.4 Reset and Miscellaneous Signals



Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[17:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • CFG[1:0]: Reserved configuration lane. • CFG[2]: S-Processor Line	I	GTL	SE	S-Processor Line P-Processor Line M-Processor Line

619501-adl-processor-eds-vol1-rev0p7

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 006_CPU (SVID/CLK/XDP/FIVR/THER

Size: A3 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 6 of 105

Main Func = CPU

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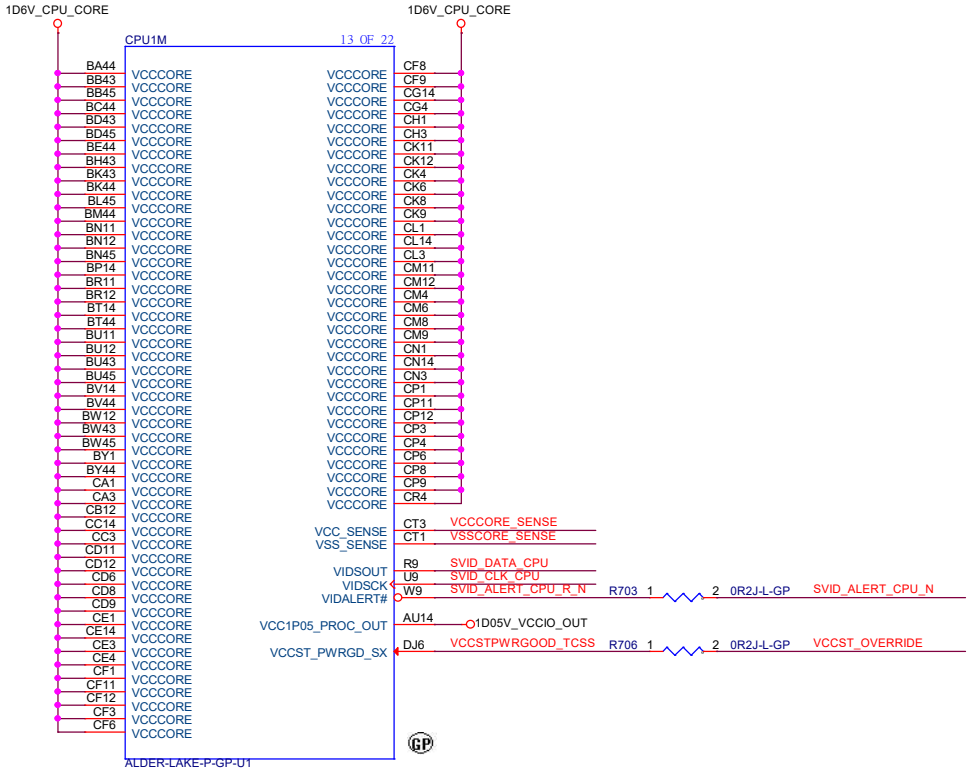
46 VCCCORE_SENSE
46 VSSCORE_SENSE
17,40 VCCST_OVERRIDE
46 SVID_ALERT_CPU_N
46,97 SVID_CLK_CPU
46 SVID_DATA_CPU



Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

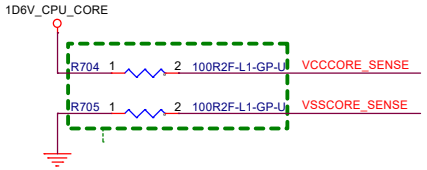


Table 750. Package Sensing Recommendations

Power Rail Sense Line	R1,R2	Trace Impedance	Trace Length Match
Vcc_SENSE /Vss_SENSE			
Vcc_{GT}_SENSE / Vss_{GT}_SENSE	100 Ohm	50 Ohm	<25 mils
Note: 1. Does not apply when rails are merged.			

To minimize any stray noise pickup to the Vcc_SENSE/ Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 25-mil separation distance away from any other dynamic signals

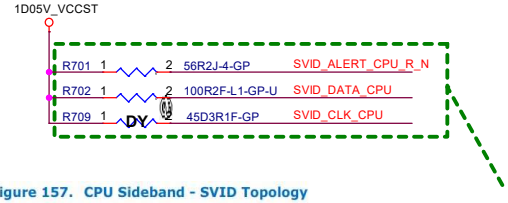


Figure 157. CPU Sideband - SVID Topology

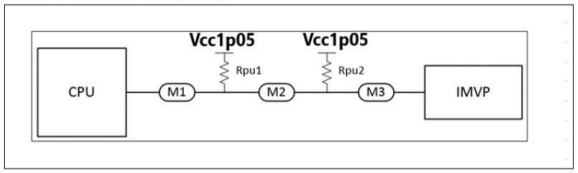


Table 341. SVID Topology Notes

Note	Detail
SVID signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=EmptyΩ
Platform resistor tolerance	± 5%
Route ordering	When routing at minimum spacing route Alert betweeen Data and Clock
Length matching between VIDSOUT and VIDSCK	± 2.54mm
Isolation Guidelines	Coupling length < 13mm. Spacing : MS = 125 um ; SL = 125 um. Coupling length < 65mm. Spacing : MS = 254 um ; SL = 250 um. Coupling length >65mm. Spacing : MS = 375 um ; SL = 300 um.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 007_CPU (VCCIN)
Size: A3
Document Number: Odin ADL-P
Rev: SC
Date: Thursday, August 05, 2021
Sheet: 7 of 105

Main Func = CPU

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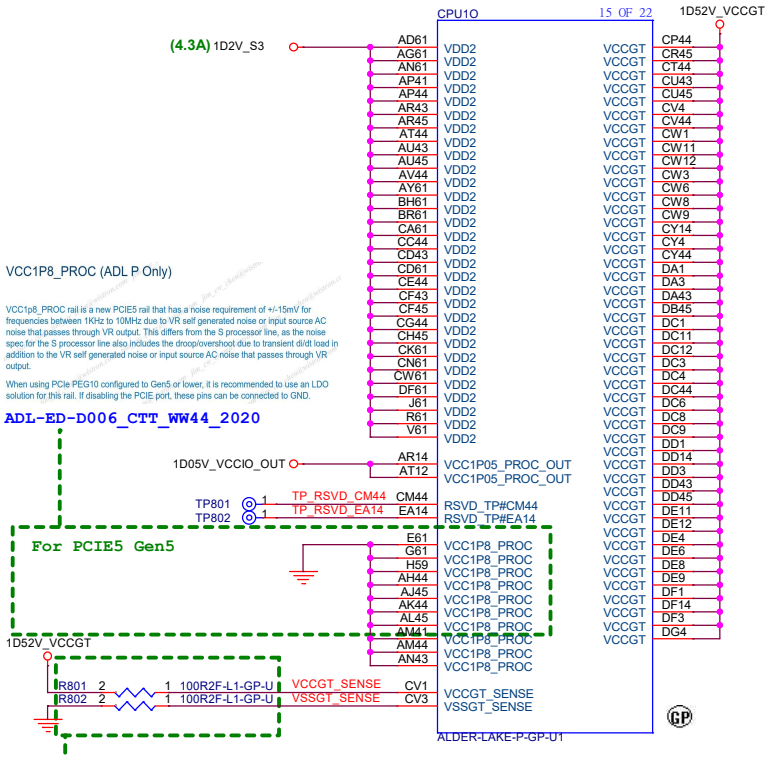
46 VCCGT_SENSE <<<—
46 VSSGT_SENSE <<<—



Layout Note:

1. VCCGT_SENSE/ VSSGT_SENSE impedance=50 ohm
2. Length match<25mil

Table 750. Package Sensing Recommendations

Power Rail Sense Line	R1,R2	Trace Impedance	Trace Length Match
Vcc_SENSE /Vss_SENSE	100 Ohm	50 Ohm	<25 mils
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Note: 1. Does not apply when rails are merged.			

To minimize any stray noise pickup to the Vcc_SENSE/ Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 25-mil separation distance away from any other dynamic signals

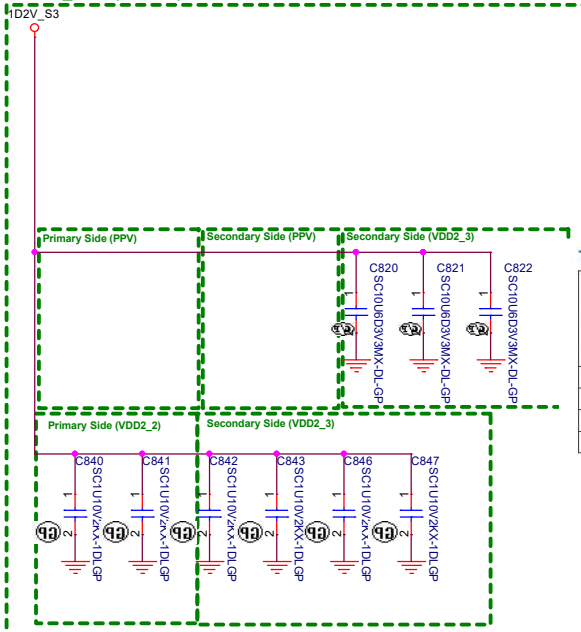
+VCC1P8_PROC (IccMax) : 100mA

Primary Side or Secondary Side (VCC1P8_PROC_3)

Table 770. Decoupling Solution

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary or Secondary Side	0402	1uF	1	Place 1uF or required value at the LDO output for stability as require by LDO vendor or datasheet. Please ensure the design is stable.	VCC1P8_PROC_3
Primary or Secondary Side	0402	10uF	1	Place directly under inner pins near pin AM41. If using a single sided solution, this capacitor maybe placed near pin E61. instead.	VCC1P8_PROC_3
Primary or Secondary Side	0402	10uF	2	Place at the input of the LDO to supress input noise between 1 to 10MHz.	VCC1P8_PROC_3
Primary or Secondary Side	0603	Placeholder	2	Placeholder as shown in reference figure.	VCC1P8_PROC_3

+VDD2_CPU (IccMax) : 2.57A



EMC CAPS:

PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART

NOTE:

PPV caps are for HVM testing only

Table 780. Decoupling Solution

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary Side	0402	1 uF	2	Place closer to outer edge VDD2 pins	VDD2_2
Secondary Side	0402	placeholder	2	Place closer to the inner row VDD2 pins	VDD2_3
Secondary Side	0402	10uF	3	Place closer to the inner row VDD2 pins	VDD2_3
Secondary Side	0402	1uF	4	Place closer to the inner row VDD2 pins	VDD2_3

+VCC1P05_OUT

Primary Side (VCC1P5_3)

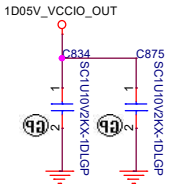


Table 768. Decoupling Solution

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary Side	0402	1uF	2	Place as close to the pins as possible	VCC1P05_3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 008_CPU (VCCIN_AUX/VCCST/VCCSTG

Size	Document Number	Rev
A3	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 8 of 105

Main Func = CPU

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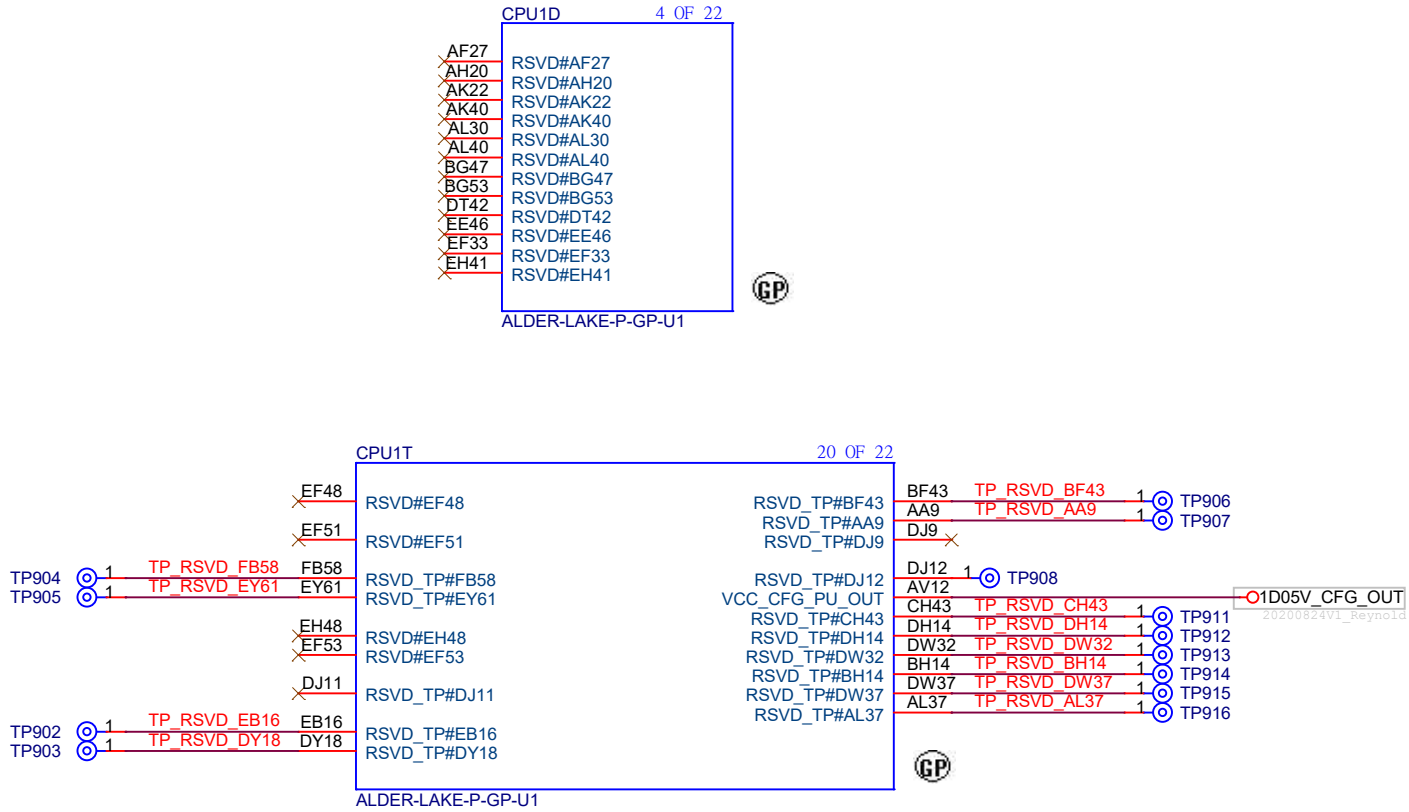


<Core Design>

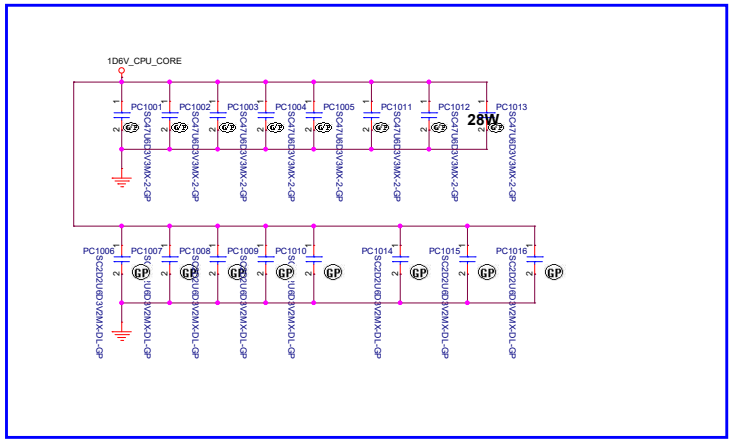
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*009_CPU (VSS)*	
Size: A4	Document Number: **Odin ADL-P**	Rev: **SC**
Date: Thursday, August 05, 2021	Sheet 9 of 105	

https://vinafix.com

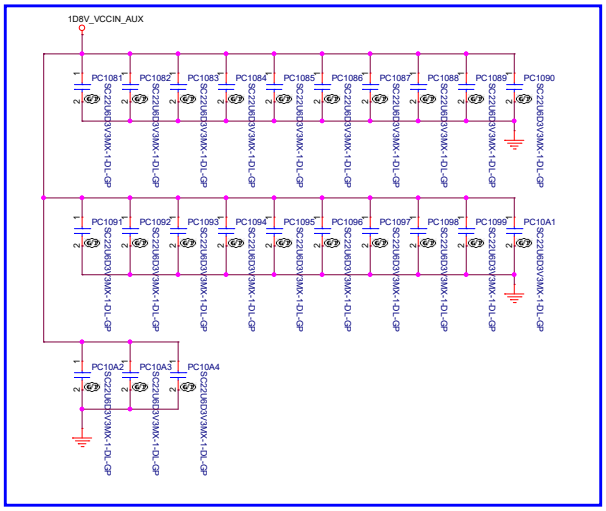
VCCIN

7*47uF 0603 + 8*2.2uF 0402 MLCC for ADL-P U15 baseline
8*47uF 0603 + 8*2.2uF 0402 MLCC for ADL-P U28 baseline



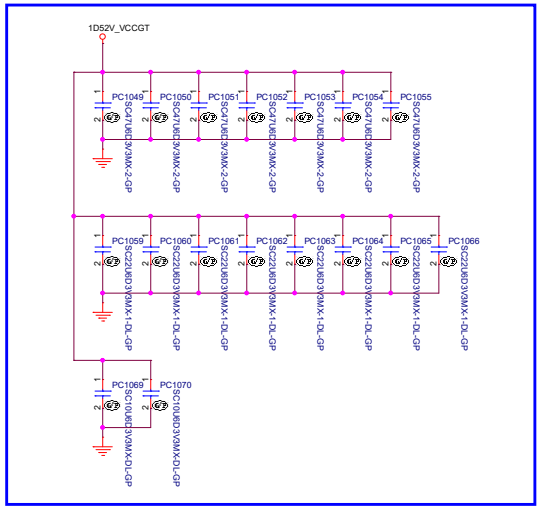
VCCIN_AUX

23*22uF MLCC for ADL-P U28 baseline



VCCGT

7*47uF + 8*22uF + 2*10uF MLCC for ADL-P U28 baseline



<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 10 of 105

Main Func = CPU

https://vinafix.com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 011_CPU (STRAP)

Size: A4 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 11 of 105

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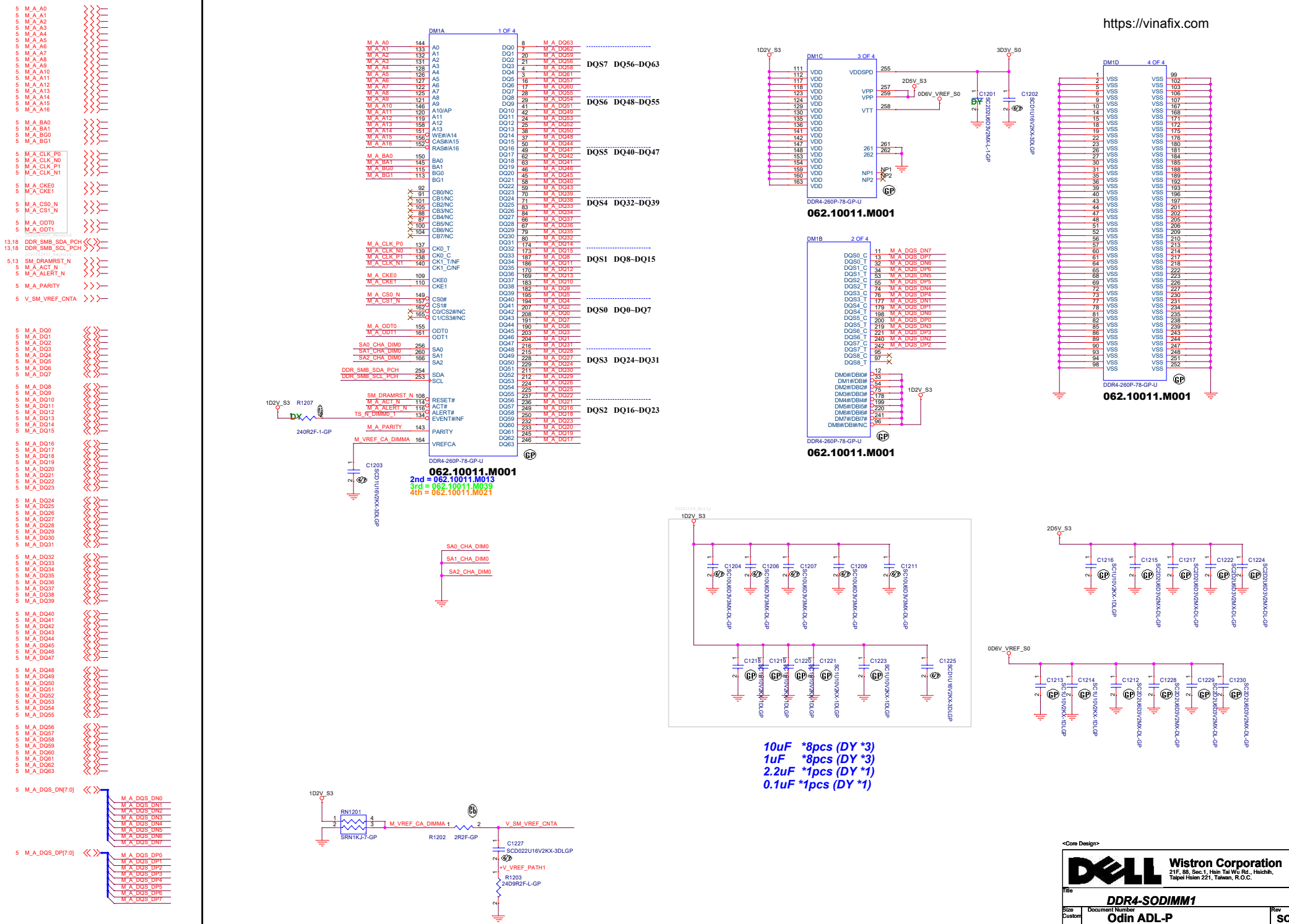

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4-SODIMM1

Size	Document Number	Rev
Custom	Odin ADL-P	SC

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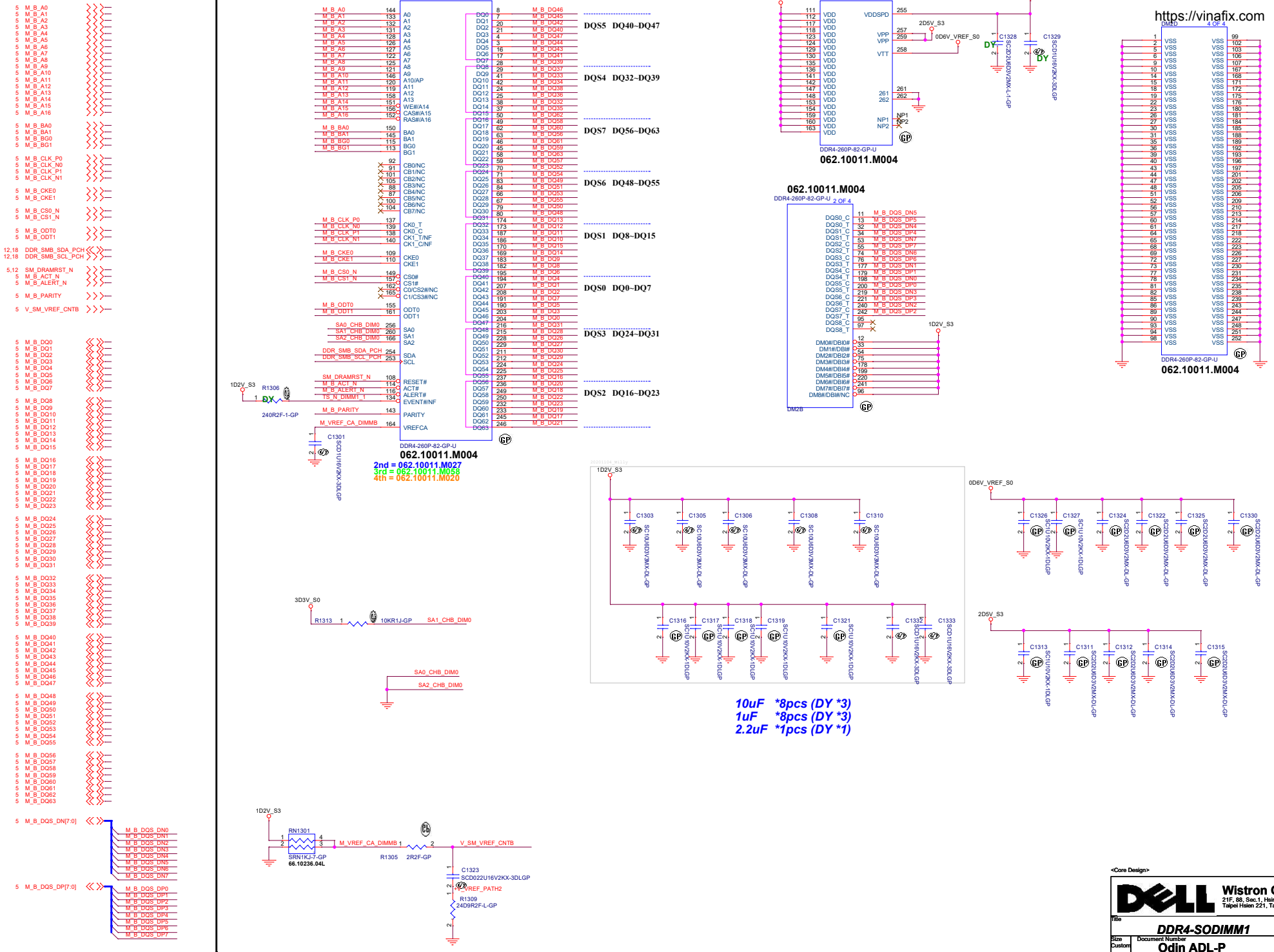
https://vinafix.com



Main Func = Memory

https://vinafix.com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 014_DDR (RSVD) (DDR4-CHA1)

Size: A4 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 14 of 105

Main Func = PCH

GPP_B14 GPP_B14 GPP_B14

GPIO	GPP_B14 Top Swap Override	SPI0_MOSI Reserved	GPP_E6 JTAG ODT Disable	GPP_F0 XTAL Frequency Selection	SPI0_IO2 Reserved	GPP_R2 Flash Descriptor Security Override	GPP_F2 M.2 CNVi Mode Select
Schematic	~default:~ ~20k PD~	~External PH required.~ Close to BIOS1/SKT1	~NO INTERNAL PU/PD~	~WAKE INTERNAL PD 20K~	Close to BIOS1/SKT1	~WAKE INTERNAL PD 20K~ * PH as VCCGPPR MP to DY	~NO INTERNAL PU/PD~
High	Enable	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Enable Override	INTEGRATED CNVI DISABLE
Low	Disable	Reserved	JTAG ODT is disabled	38.4 MHz	Reserved	Disable Override	INTEGRATED CNVI ENABLE
GPIO	GPP_E19 DDP1 I2C/TBT_LSX0/BSSB_LS0 Pins VCC configuration	GPP_E21 DDP2 I2C/TBT_LSX1/BSSB_LS1 Pins VCC configuration	GPP_D10 DDP3 I2C/TBT_LSX2/BSSB_LS2 Pins VCC configuration	GPP_D12 DDP4 I2C/TBT_LSX3/BSSB_LS3 Pins VCC configuration	SPI0_IO3 Reserved	DBG_PMODE Reserved	GPP_B18 No Reboot
Schematic	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~ Close to BIOS1/SKT1		~20 kohm ± 30% internal pull-up~	~WAKE INTERNAL PD 20K~
High	3.3V	3.3V	3.3V	3.3V	Reserved	Reserved	Enable "No Reboot" mode
Low	1.8V	1.8V	1.8V	1.8V	Reserved	Reserved	REBOOT ENABLED
GPIO	GPD7 Reserved	GPP_C2 TLS Confidentiality	GPP_B23 CPUNSSC Clock Frequency	SPIVCCIOSEL SPI Operation Voltage Select	GPP_F7 Reserved	GPP_F10 Reserved	
Schematic	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	~External PH required.~	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	
High	Reserved	Enable	19.2MHz	1.8V	LDO BYPASS	Reserved	
Low	Reserved	Disable	38.4MHz	3.3V	NO BYPASS	Reserved	
GPIO	GPP_C5 Boot Strap 0	GPP_H0 Boot Strap 1	GPP_H1 Boot Strap 2	GPP_H2 Boot Strap 3			
Schematic	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~	~WAKE INTERNAL PD 20K~			
High	Reserved	Reserved	Reserved	Reserved			
Low	Reserved	Reserved	Reserved	Reserved			

This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled
0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Original Ref.

GPIO	GPP_B14/SPKR TOP SWAP OVERRIDE	SPI0_MOSI	GPP_E6 JTAG ODT Disable	GPP_F0 XTAL Freq Selection	SPI_IO_2 SPI_WP_CPU	GPP_R2 / HDA_SDO Flash Security Override	GPP_F2 / CNV_RGI_DT M.2 CNVi Mode Select
Schematic							
High	Enable	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Enable Override	INTEGRATED CNVI DISABLE
Low	Disable	Reserved	JTAG ODT is disabled	38.4 MHz	Reserved	Disable Override	INTEGRATED CNVI ENABLE
GPIO	GPP_E19/NC TBT_LSX0_VCC config	GPP_E21/USB1_TCSS_RXD TBT_LSX1_VCC config	GPP_D10/USB2_TCSS_RXD TBT_LSX2_VCC config	GPP_D12/NC TBT_LSX3_VCC config	SPI_IO_3 SPI_MOSI_CPU	DBG_PMODE	GPP_B18 No Reboot
Schematic							
High	3.3V	3.3V	3.3V	3.3V	Reserved	Reserved	Enable "No Reboot" mode
Low	1.8V	1.8V	1.8V	1.8V	Reserved	Reserved	REBOOT ENABLED
GPIO	GPD_7	GPP_C2/SMBALERT# CSME Crypto TLS	GPP_B23/GPP_B23_CLK_SEL CPUNSSC Clock Frequency	SPIVCCIOSEL	GPP_F7/MCRO_LDO_ BYPASS	GPP_F10/LAN_RST_N	
Schematic							
High	Reserved	Enable	19.2MHz	1.8V	LDO BYPASS	Reserved	
Low	Reserved	Disable	38.4MHz	3.3V	NO BYPASS	Reserved	
GPIO	GPP_C5 GPP_C5 BOOT STRAP0	GPP_H0/GPP_H0_BOOT_STRAP1 Boot Strap 1	GPP_H1/GPP_H1_BOOT_STRAP2 Boot Strap 2	GPP_H2/GPP_H2_BOOT_STRAP3 Boot Strap 3			
Schematic							
High	Reserved	Reserved	Reserved	Reserved			
Low	Reserved	Reserved	Reserved	Reserved			

Table 16. Pin Straps

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR / TIME_SYNC1 / SATA_LED# / ISH_GP6	Top Swap Override	Rising edge of PCH_PWROK	This strap has a 20 kohm ± 30% internal pull-down. 0=>Disable "Top Swap" mode. (Default) 1=>Enable "Top Swap" mode. This inverts an address on access to SPI, so the alternate boot block is fetch instead of the original boot-block. The PCH will invert A16 (default) or the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap. *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / ADR_COMPLETE	No Reboot	Rising edge of PCH_PWROK	This strap has a 20 kohm ± 30% internal pull-down. 0=>Disable "No Reboot" mode. (Default) 1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_C5 / SMLOALERT#	Boot Strap 0	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.

continued...

Signal	Usage	When Sampled	Comment
GPP_R2 / HDA_SDO / I2S2_TXD / HDACPU_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This strap has a 20 kohm ± 30% internal pull-down. 0=> Enable security measures. (Default) 1=> Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E6 / THC0_SPI1_RST#	JTAG ODT Disable	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. External pull-up is recommended 0=> JTAG ODT is disabled 1=> JTAG ODT is enabled
GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD / BSSB_LS0_TX	DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8 V 1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3 V *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD / BSSB_LS1_RX	DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8 V 1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3 V *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
DBG_PMODE	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-up. This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling. *Notes:* 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / BSSB_LS2_TX / GSPI2_CLK	DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8 V 1 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3 V *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_D12 / ISH_SPI_MOSI / DDP4_CTRLDATA / TBT_LSX3_RXD / BSSB_LS3_TX / GSPI2_MOSI	DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 1.8 V 1 = DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 3.3 V *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPD7	Reserved	Rising edge of DSW_PWROK	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. *Notes:* 1. The internal pull-down is disabled after DSW_PWROK is high. 2. This signal is in the DSW well.
GPP_F0 / CNV_BRI_DT / UART2_RTS#	XTAL Frequency Selection	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = 38.4 MHz (default) 1 = 24 MHz *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F2 / CNV_RGI_DT / UART2_TXD	M.2 CNVi Mode Select	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled. *Note:* When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

continued...

Signal	Usage	When Sampled	Comment
GPP_B23 / SML1ALERT# / PCHHOT#	CPUNSSC Clock Frequency	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = 38.4 MHz clock (direct from crystal) (default) 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150 K pull-up is needed to ensure it does not override the internal pull-down strap sampling. 3. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

continued...

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Wistron Corporation
Taipei Hsien 221, Taiwan, R.O.C.

Title: 015_DDR (RSVD) (DDR4-CHB1)
Size: C
Project: Odin ADL-P
Rev: SC
Date: Monday, May 16, 2022
Sheet 15 of 135

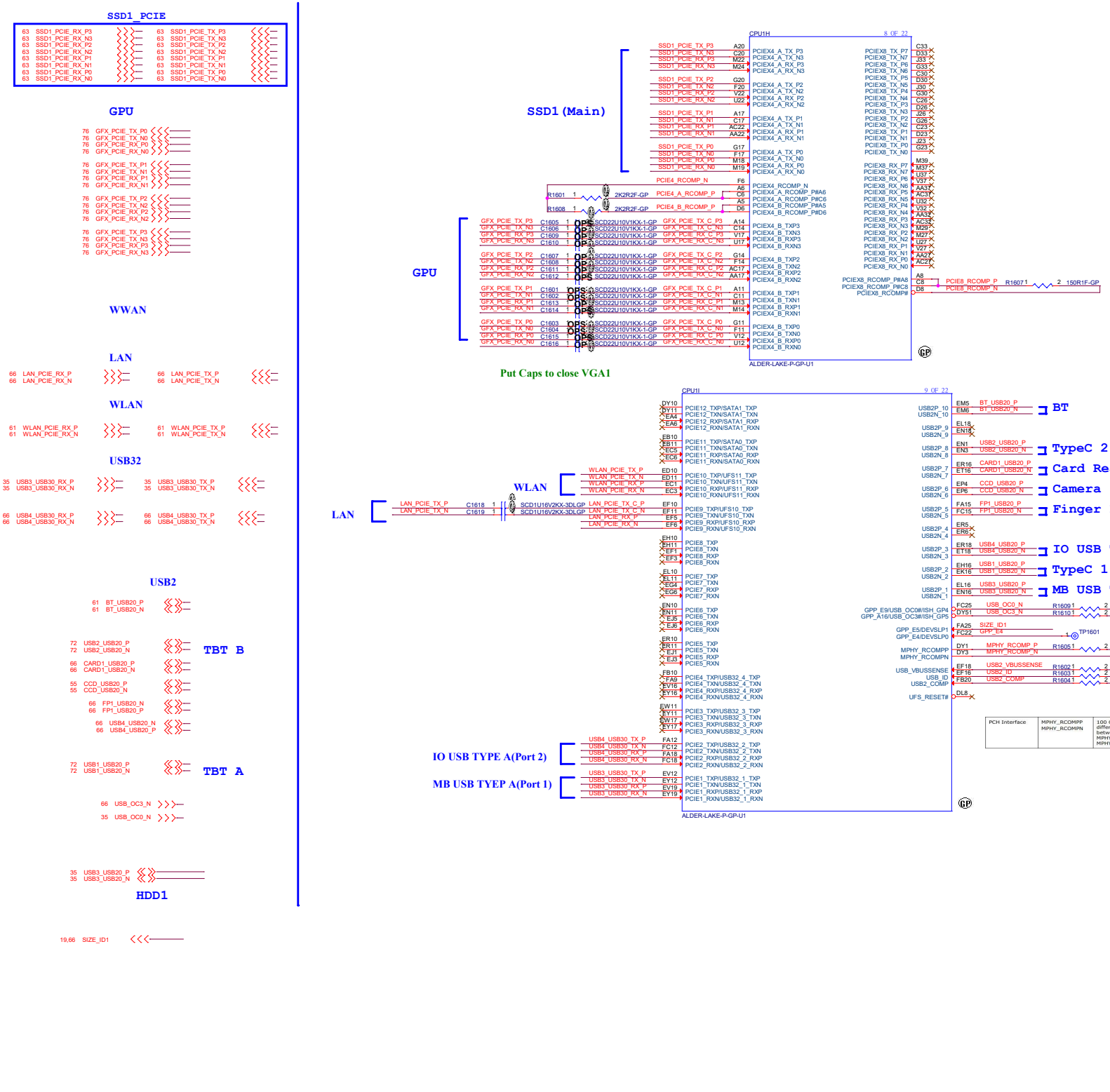

Table 308. PCI Express* Signal Groups

Interface	Signal Group	Signal Name	Description
PCIe x8 Gen5	Input PCI Express*	PCIEX8_RX_N [7:0] PCIEX8_RX_P [7:0]	Gen 5 PCI Express* Receive Differential Pair
	Output PCI Express*	PCIEX8_TX_N [7:0] PCIEX8_TX_P [7:0]	Gen 5 PCI Express* Transmit Differential Pair
	COMP	PCIE_X8_RCOMP_P PCIE_X8_RCOMP_N	Gen 5 PCI Express* Compensation
PCIe x4 Gen4	Input PCI Express*	PCIEX4_A_RX_P[3:0] PCIEX4_A_RX_N[3:0]	Gen 4 PCI Express* Receive Differential Pair
	Output PCI Express*	PCIEX4_A_TX_P[3:0] PCIEX4_A_TX_N[3:0]	Gen 4 PCI Express* Transmit Differential Pair
	COMP	PCIE_X4_A_RCOMP_P PCIE_X4_RCOMP_N	Gen 4 PCI Express* Compensation
PCIe x4 Gen4	Input PCI Express*	PCIEX4_B_RX_P[3:0] PCIEX4_B_RX_N[3:0]	PCI Express* Receive Differential Pair
	Output PCI Express*	PCIEX4_B_TX_P[3:0] PCIEX4_B_TX_N[3:0]	PCI Express* Transmit Differential Pair
	COMP	PCIE_X4_B_RCOMP_P PCIE_X4_RCOMP_N	PCI Express* Compensation

Interface	Pin Name	Board Rterm (Ohm)	Board DC resistance (ohms)	Board parasitic capacitance (pF)	Notes
PCIe	PCIE_X8_RCOMP_P	150 Ohms with 1% end of life precision between p and n	Loop of P and n should < 0.0625 ohms	Not applicable. Make as wide as possible to reduce Rdc.	
PCIe	PCIE_X8_RCOMP_N			0.92pF for N only	
PCIe	PCIE_X4_A_RCOMP_P	2.2k +/- 0.1% between P and N	0.05	1.04	
PCIe	PCIE_X4_RCOMP_N				

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6.9.2 USBCOMP Connection Guidelines

- Short the USB2_COMP pins at the package and then route on the top layer to one end of a 113 Ω ±1% resistor to ground.
- Route signal using 50 Ω single-ended impedance and 12.7-mm max trace length and no longer than 11.43mm to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 0.381mm.

6.9.3 USBCOMP Routing Guidelines

Table 486. USBCOMP Routing Guidelines

Signal	Trace Width (W) and Isolation Spacing (S)	Resistor Value	Length
USB2_COMP	No hard value for trace width and isolation spacing as long as DCR is met *Note:* : Must maintain low DC resistance routing (< 0.5Ω)	113 Ω ± 1% connected to GND	M1/M1' + M2

Notes: 1. Although there is no hard value for max topology length as long as the DC resistance routing spec is met, although it is recommended to route the USB2_COMP using 50 single-ended impedance and as short as possible; a general recommendation is to maintain a length of <25.4mm, which will make it easier to hit the targeted DCR.
2. Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 0.381mm

6.9.4 USB2_COMP to Other Interfaces

If unable to implement a Vss shield for USB2_COMP, the minimum spacing between USB2_COMP and other traces should be at least 0.381mm to provide proper isolation.

If Vss shielding is implemented, then the spacing guideline in the figure below should be followed:

Main Func = PCH

53,97 PM_SLP_SUS_N
51,66,97 PM_SLP_S4_N
40,55,97 PM_SLP_S3_N
24,97 PM_PWRBTN_N
15 GPD_7
24 LAN_WAKE_N
24,97 SYS_PWROK
72 CPU_PMC_ALERT_N
46 PWR_VCORE_VR_READY — PWR_VCORE_VR_READY
24 PCH_DPWROK
40,97 ALL_SYS_PWRGD
15 SPI_VCC_SEL
7,40 VCCST_OVERRIDE
97 CPU_C10_GATE_N
64,97 PM_RSMRST_N
24 EC_RSMRST_N
63,66,71,75,76,91,97 PLT_RST_N
44 AC_IN#
19 TPM_PRSNT#
25,45 3V_5V_POK
24 EC_PCH_SPI_EN
97 CPU_PWRGD
97 AC_PRESENT
97 PM_SLP_S5_N
97 DSW_PWROK_R
97 VCCST_PWRGD
97 PCH_PWROK
19 VRAM_ID2
19 PROJECT_ID3
24,26,40 IMVP_VR_ON

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PM_SLP_SUS_N	EN53	SLP_SUS#	
PM_SLP_S5_N	EG60	GPD10/SLP_S5#	GPD : 3.3V
PM_SLP_S4_N	EP56	GPD5/SLP_S4#	GPD : 3.3V
PM_SLP_S3_N	EM59	GPD4/SLP_S3#	GPD : 3.3V
PM_SLP_A_N	EM57	GPD6/SLP_A#	GPD : 3.3V
PM_SLP_WLAN_N	EJ57	GPD9/SLP_WLAN#	GPD : 3.3V
PM_SLP_S0_N	DW59	GPP_B12/SLP_S0#	
PM_SLP_LAN_N	EK53	SLP_LAN#	
PM_RSMRST_N	EH53	RSMRST#	
SYS_RESET_N	EK26	SYS_RESET#	
PLT_RST_N	DW57	GPP_B13/PLTRST#	
DSW_PWROK_R	EE48	DSW_PWROK	
SYS_PWROK	EK23	SYS_PWROK	
PCH_PWROK	EH51	PCH_PWROK	
RTC_INTRUDER_N	DY44	INTRUDER#	
SPI_VCC_SEL	EL53	SPIVCCIOSEL	
CPU_PWRGD	BG11	PROCPWRGD	

GPD3/PWRBTN#	EM61	PM_PWRBTN_N	
GPD0/BATLOW#	EM56	PM_BATLOW_N	
GPD1/ACPRESENT	EJ59	AC_PRESENT	
GPP_B11/PMCALERT#	EA56	CPU_PMC_ALERT_N	
GPP_H18/PROC_C10_GATE#	ER46	CPU_C10_GATE_N	
GPP_H3/SX_EXIT_HOLDOFF#	ET48	TPM_PRSNT#	
WAKE#	ET51	PCH_WAKE_N	
GPD2/LAN_WAKE#	EP58	LAN_WAKE_N	
GPD11/LANPHYPC	EJ56	LANPHYPC	
GPD7	EK60	GPD_7	
VRAM_ID2	FA22	VRAM_ID2	
PCH_PWROK	DK5	PCH_PWROK	
VCCST_OVERRIDE	DK4	VCCST_OVERRIDE	
PROJECT_ID3	EH28	PROJECT_ID3	
GPP_F20/EXT_PWR_GATE#	EH31		
GPP_F21/EXT_PWR_GATE2#			

TP1702 — TP1701 — TP1703

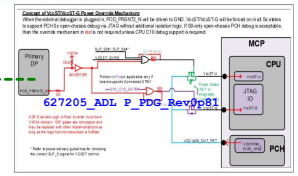
3D3V_S5_PCH

R1716 1 DY 2 10KR2F-2-GP LAN_WAKE_N
R1762 1 DY 2 10KR2F-2-GP CPU_PMC_ALERT_N
R1712 1 DY 2 10KR2F-2-GP PCH_WAKE_N
R1706 1 DY 2 100KR2J-1-GP AC_PRESENT
R1707 1 DY 2 10KR2F-2-GP PM_BATLOW_N
R1761 1 DY 2 100KR2J-1-GP PM_SLP_S0_N
R1713 1 2 10KR2F-2-GP SYS_RESET_N

Table 371. Signals Required Pull-up Resistor

Signal Name	Pull-Up Resistor Value		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
GPP_B11 / SLP_S0# GPP_F22 / EXT_PWR_GATE# GPP_F21 / EXT_PWR_GATE2#	100K 100K 100K	75K 75K 75K	Pull-up resistor is required on GPP_B11 / SLP_S0# if a device is connected to the platform. EXPRESS-P: Be aware of

Figure 574. VCCST and VCCST-G Override



power supplies are stable
ROC power on when needed

R1749 1 100KR1J-GP PM_SLP_WLAN_N
R1748 1 100KR1J-GP PM_SLP_A_N
R1747 1 100KR1J-GP PM_SLP_S3_N
R1746 1 100KR1J-GP PM_SLP_S4_N
R1745 1 100KR1J-GP PM_SLP_S5_N
R1790 1 100KR1J-GP PM_SLP_SUS_N
R1791 1 100KR1J-GP PM_SLP_S0_N
R1718 1 100KR1J-GP CPU_C10_GATE_N
R1714 1 100KR1J-GP SYS_PWROK
R1719 1 100KR1J-GP PLT_RST_N
R1705 1 100KR1J-GP PCH_PWROK
R1741 1 100KR1J-GP PM_RSMRST_N

Table 369. Signals Required Cap or Pull-Down Resistor

Signal Name	Option 1 (Cap Implementation)		Option 2 (Pull-down Resistor Implementation)		Note
	3.3v Ramp Rate from 5-50ms	3.3V Ramp Rate Less than 5ms	3.3V Signaling Mode	1.8V Signaling Mode	
GPD4 / SLP_S3# GPD5 / SLP_S4# GPD6 / SLP_A# GPD9 / SLP_WLAN#	330 nF	33 nF	100 K	N/A	Cap or pull-down resistor is required
SLP_SUS# SLP_LAN#	330 nF	33 nF	100 K	N/A	
SPI0_CLK GPP_H18 / PROC_C10_GATE#	N/A	N/A	100K	75K	Pull-down resistor is required.
eDP_BKLTEN eDP_VDDEN	330 nF	33 nF	100K	75K	Cap or pull-down resistor is required depending on panel power sequencing spec or power delivery
CNV_RF_RESET#	N/A	N/A	N/A	75K	Pull-down resistor to ensure the stability of the signal during platform bootup

627205_ADL P_PDG_Rev0p7

SCD1U16V2KX-3DLGP C1714 — 3D3V_S5

EC_RSMRST_N R17731 2 0R1J-GP EC_RSMRST_N_U 2
PCH_DPWROK R17751 2 0R1J-GP PCH_DPWROK_R 3
3D3V_S5_R R17711 2 0R1J-GP 3D3V_S5_U 4

U1703
VDD
PCH_RSMRST#
PCH_DPWROK
DSW_PWROK
3V_5V_PWRGD 8 — 3V_5V_PWRGD_U — R17721 2 0R1J-GP 3V_5V_POK
NC#7 7
EC_PCH_SPI_EN 6 — EC_PCH_SPI_EN_R — R17741 2 0R1J-GP EC_PCH_SPI_EN
GND 5
SLG4E43789VTR-1-GP
074.43789.M001
2nd = 074.03904.0053

RSMRST#

PM_SLP_SUS_N — R1711 0R2J-2-GP — PM_SLP_SUS_AND — U1702 — DSW_PWROK_R
3D3V_S5 — C1703 SCD1U16V2KX-3DLGP — DSW_PG_R — R1709 0R2J-2-GP — DSW_PG
TC7SZ08FU-LJ-C-GP
073.7SZ08.000G
2nd = 73.7SZ08.DAH
3rd = 73.01G08.L04

DSW_PG — U1705 — EC_RSMRST_N
3D3V_S5 — C1721 SCD1U16V2KX-3DLGP — PM_RSMRST_N_R — R1724 0R2J-2-GP — PM_RSMRST_N
C1722 SCD1U16V2KX-3DLGP
RC_delay 10ms
TC7SZ08FU-LJ-C-GP
073.7SZ08.000G
2nd = 73.7SZ08.DAH
3rd = 73.01G08.L04

From EC Control

3D3V_S5_PCH — R1708 2K2R1J-GP — DSW_PWROK_R — R1710 0R2J-L-GP — PCH_DPWROK
R1704 100KR2J-1-GP — C1702 SCD01U25V2KX-1-GP
Delay 3D3V_S5 over 10ms.
Delay 3D3V_B_S5 after 25ms.

3D3V_S5 — U1701 — ALL_SYS_PWRGD
NC#1 VCC 5 — C1701 SCD1U16V2KX-3DLGP — 1D05V_VCCST — R1702 1KR2F-3-GP
A 2
GND 3 — Y 4 — VCCST_PWRGD_R — R1701 62R2F-GP — VCCST_PWRGD
74LVC1G07GW-GP
73.01G07.0HG
2nd = 073.7SZ07.000G
3rd = 73.17S07.0AG

PM_SLP_S3_N — D1704 — A — RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

PCH_PWROK

3D3V_S0 — R1737 10KR1J-GP — PWR_VCORE_VR_READY — R1743 1 2 0R1J-GP — PCH_PWROK
From PWR_VCCIN_VRRDY

PM_SLP_S3_N — R1794 0R1J-GP — D1703 — A — RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F
IMVP_VR_ON — R1795 0R1J-GP

RTC_AUX_S5 — R1715 1MR2F-GP — RTC_INTRUDER_N

1.8 RTC Circuit Checklist
Table 16. RTC Checklist

Rtn Name:	Notes:	✓
RTCX1, RTCX2	Connect a 32.768 kHz crystal oscillator across these pins with a 20 pF load capacitor and 10 MΩ resistor. Values for C1 and C2 are dependent on crystal vendor recommended value. Typical values of C1 and C2 are 18 pF, based on a crystal load of 12.5 pF.	✓ with 12 pF.
RTCRST#	An RC delay circuit with a time delay in the range of 19-23 ms. should be provided. The recommended values for resistor and capacitor are 20 MΩ and 1.0 µF. The circuit should be placed close to the PCH.	✓
SRTCRST#	An RC delay circuit with a time delay in the range of 19-23 µs. should be provided. ONE uses 20 MΩ and 1.0 µF for resistor and capacitor. The circuit should be placed close to the PCH.	✓
INTRUDER#	1. A 15kΩ pull-up is used on the customer reference board (CRB). This is needed to reduce leakage from the Coin Cell battery in S3 level.	✓

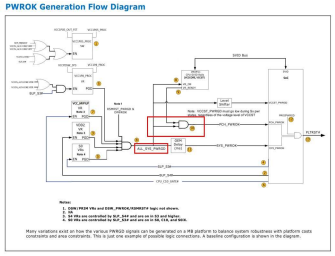
Note: For further information on the RTC, refer to the Real Time Clock Section in RDG.

83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

AC_PRESENT

3D3V_AUX_S5 — R1735 100KR1J-GP — PM_RSMRST_M_N — Q1702 2N7002KDW-1-GP — PM_RSMRST_R_N — R1734 0R1J-GP — PM_RSMRST_N
D1701 RB520S30-GP — AC_IN#
AC_PRESENT
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C
Reserve by NON DS3 function 20150413

Figure 499. PWROK Generation Flow Diagram



PCH_PWROK			VR_READY (Generated from IMVP9.1 VR) should be logical AND with ALL_SYS_PWRGD.	PWR_VCCIN_VRRDY AND with ALL_SYS_PWRGD PM_SLP_S3_N (DY)

627205_ADL P_SchChk_Rev0p8

3D3V_S5 — 3D3V_S5_PCH
R1720 390KR2J-GP — 3D3V_S5_PCH_R — U1704 — 3D3V_S5
R1792 100KR2J-1-GP — 3D3V_S5_R — DSW_PWROK_R
3V_5V_POK — D1793 — A — RB520S30-GP
C1713 SCD1U16V2KX-3DLGP
TC7SZ08FU-LJ-C-GP
073.7SZ08.000G
2nd = 073.7SZ08.DAH
3rd = 73.01G08.L04
2nd = 083.52030.008F
83.R2003.A8M

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 017_PCH (PCIE/SATA/RTC)
Size: A2 | Document Number: Odin ADL-P | Rev: SC
Date: Thursday, August 05, 2021 | Sheet 17 of 106

Main Func = PCH

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R1

R1807 R1811 R1810 R1809 R1808	
TPM	0R 63.R003C.1IL
NON TPM	15R 63.15034.1DL

SPI

24,25,68,91 SPI_CLK_ROM
24,25,68 SPI_HOLD_ROM
24,25,68 SPI_WP_ROM
24,25,68,91 SPI_SO_ROM
24,25,68,91 SPI_SI_ROM
24,25,68 SPI_CS_CPU_N0

15,68 SPI_HOLD_CPU
15,68 SPI_WP_CPU
15,68 SPI_SI_CPU

68 SPI_CLK_CPU
68 SPI_SO_CPU
68 SPI_CS_CPU_N0_R

97 RTC_RST_N
97 SRTC_RST_N
19 AUDIO_DET

DDR

12,13 DDR_SMB_SDA_PCH
12,13 DDR_SMB_SCL_PCH

BB

71,75 CPU_SMB_SCL_P0
71,75 CPU_SMB_SDA_P0

PD

72 CPU_SMB_SCL_P1
72 CPU_SMB_SDA_P1

ESPI

24 ESPI_CPU_CLK
24 ESPI_CPU_IO3
24 ESPI_CPU_IO2
24 ESPI_CPU_IO1
24 ESPI_CPU_IO0
24,68 ESPI_CPU_CS_N
24,68,97 ESPI_CPU_RST_N

GFX

76 GFX_CLK_CPU_P
76 GFX_CLK_CPU_N
76 GFX_CLKREQ_CPU_N

WLAN

61,97 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N

WWAN

LAN

66 LAN_CLK_CPU_P
66 LAN_CLK_CPU_N
66 LAN_CLKREQ_CPU_N

SSD1

63 SSD1_CLK_CPU_P
63 SSD1_CLK_CPU_N
63 SSD1_CLKREQ_CPU_N

91 SPI_CS_CPU_N2

55 TOUCH_PANEL_INTR#_R

79,86 GC6_FB_EN

GPU

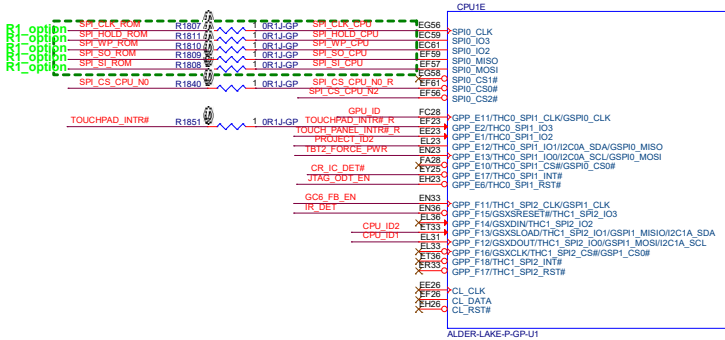
15 CPU_SMB_ALERT_N
15 GPP_B23_CLK_SEL
15 JTAG_ODT_EN
15 GPP_C5

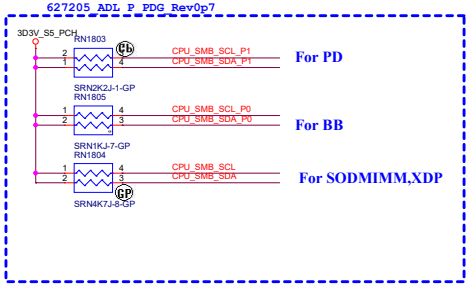
55 IR_DET
24,61,97 SUS_CLK_CPU
24 DUAL_BOOT_EVENT#
19 TBT_DET#
55 DBC_PANEL_EN
72,75 TBT2_FORCE_PWR
66 CR_IC_DET#

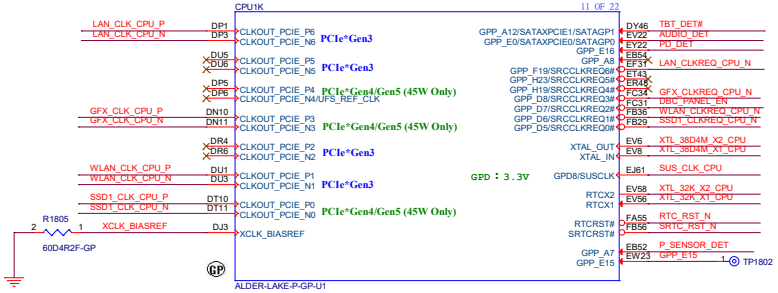
SITP

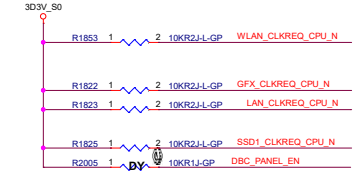
96 CPU_SMB_SCL
96 CPU_SMB_SDA

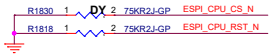
68 ESPI_CPU_IO0_DBG
68 ESPI_CPU_IO1_DBG
68 ESPI_CPU_IO2_DBG
68 ESPI_CPU_IO3_DBG
68 ESPI_CPU_CLK_DBG

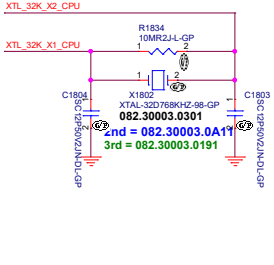


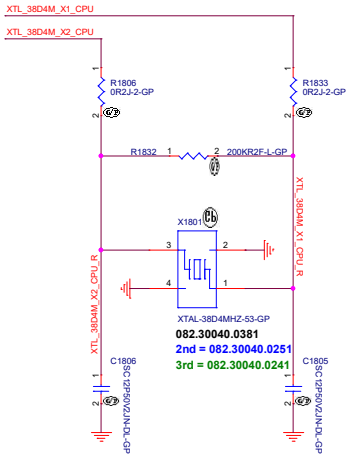


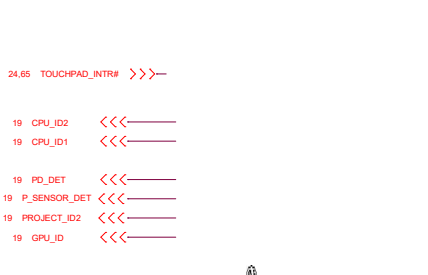


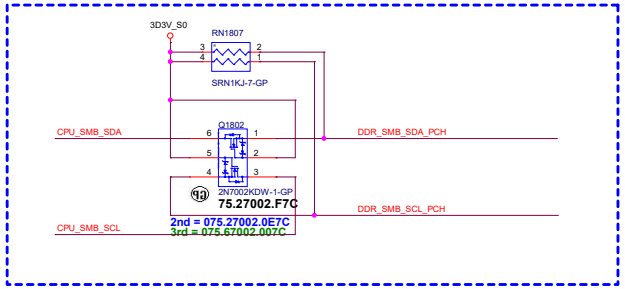












PCIe* Gen5 Serial Reference Clocks (SRCs)

- Similar usage model compared to standard differential SRC used for PCIe* Gen3 and Gen4.
- Utilize port 0, 1 and 4 for Gen5 support on their buffer is specifically designed to meet PCIe*5 lower jitter and they are inner row BGAs and are easier to breakout at bottom layer (to have full GND referencing).

ADL-ED-D005_CTT_WW44_2020

627205_ADL_P_PDG_Rev0p8

6.1.2 Signal Descriptions

Table 344. Platform Clocks and Associated Signal Details and Descriptions

Signal Name	Type	SSC Capable	Description
• CLKOUT_PCIE_P [6:0] • CLKOUT_PCIE_N [6:0]	O	Yes	PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support • CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support Any un-used CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the Intel® Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.

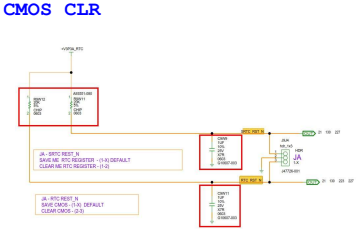
627205_ADL_P_PDG_Rev0p7

Figure 247. eSPI 1-Load Topology (Device Down) Diagram

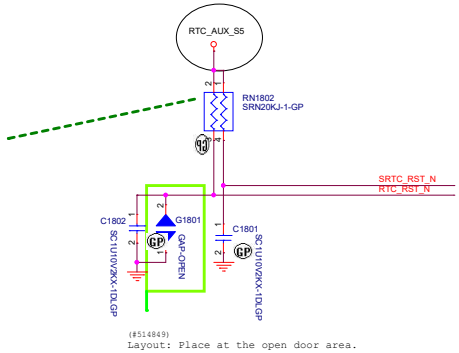
Table 511. 1-Load Topology (Device Down) Notes

Note	Detail
Number of vias allowed	7
Reference plane	Continuous ground only
Max Frequency	50MHz
Device assumption	Compliant to Intel ESPI Base Specification 1.0 (66MHz and above)
R1	33Ω on ESPI_CLK, ESPI_IO[3:0]
Minimum length	[1] R1: 12.7mm [2] M1, M2 and M4: 2.54mm
Length matching between CLK and DATA signals	12.7mm
Trace spacing between DATA and DATA signals	0.127mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	ESPI_CLK, ESPI_IO[3:0]; ESPI_CS0#

CMOS CLR



631621_ADL_P_DDR5_SODIMM_RVP_TDK_Rev0p71



(#514849)
Layout: Place at the open door area.

<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 018_PCH (USB31/USB2/SPI/XTAL)

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 18 of 106

Main Func = PCH

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Antman N 14/16 MB

	3209 SPK	2514 SPK
Vendor A	GPP_S0 pull low, GPP_S1 pull low	GPP_S0 pull high, GPP_S1 pull low
Vendor B	GPP_S0 pull low, GPP_S1 pull high	GPP_S0 pull high, GPP_S1 pull high

Antman N 14/16 SPK BD

	1609 SPK
Vendor A	GPP_S7 pull low
Vendor B	GPP_S7 pull high

Odin NV 14/16 MB

	Odin 14N, 3209 SPK	Odin 16NV, 2514 SPK
Vendor A	GPP_S1 pull low	GPP_S1 pull low
Vendor B	GPP_S1 pull high	GPP_S1 pull high

27,96 HDA_SDOUT_CODEC
27 HDA_SYNC_CODEC
27,96 HDA_BITCLK_CODEC
15,19 HDA_SDOUT_CPU
27,96 HDA_SDIN0_CPU

61 BLUETOOTH_EN
15,19 HDA_SDOUT_CPU

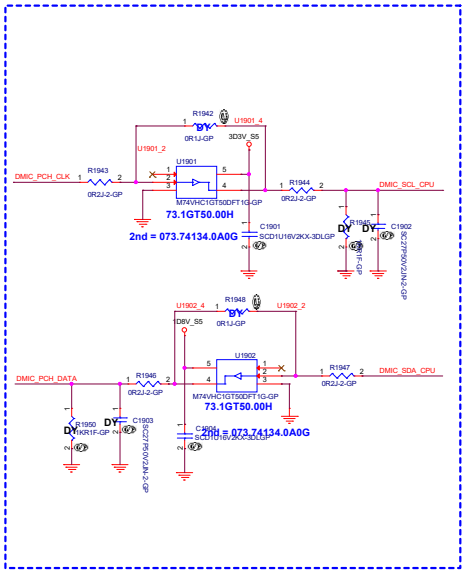
25 RTC_DET_N
91 TPM_SPI_IRQ#
86 DGPU_PWR_EN

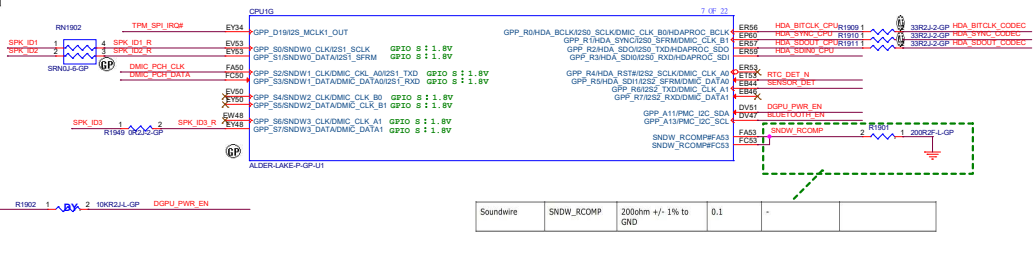
55 DMIC_SCL_CPU
55 DMIC_SDA_CPU
29 SPK_ID1
29 SPK_ID2
28 SPK_ID3

SIV Auto Test

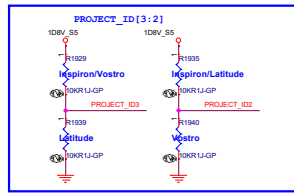
96 HDA_BITCLK_CPU

18 TBT_DET#
18 CPU_ID2
18 CPU_ID1
16,66 SIZE_ID1
18 GPU_ID
17 VRAM_ID2
21 VRAM_ID1
18 PD_DET
17 TPM_PRSNT#
18 AUDIO_DET
18 P_SENSOR_DET
17 PROJECT_ID3
18 PROJECT_ID2

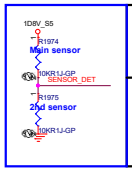




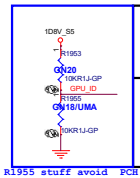
Soundwire	SNDW_RCOMP	200ohm +/- 1% to GND	0.1	-	



ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude
		00	N/A

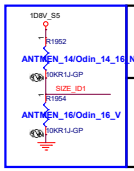


ID	Description	Setting	Mapping
SENSOR_DET	SENSOR type detected	1	LNG2DMTR LSM6DSO LIS2MDL
		0	Bosch BMA422 Bosch BMI260 BMI150

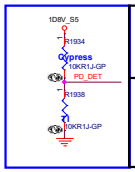


ID	Description	Setting	Mapping
GPU_ID	GPU type detected	1	GN20
		0	GN18

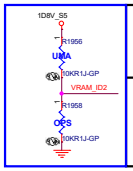
UMA R1955 stuff avoid PCH floating



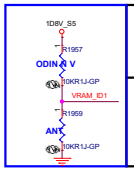
ID	Description	Setting	Mapping
SIZE_ID1	NVL Size detected	1	14 inch
		0	16 inch



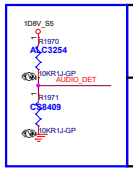
ID	Description	Setting	Mapping
PD_DET	PD function detected	1	Cypress
		0	TI



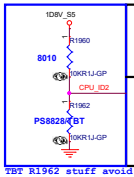
ID	Description	Setting	Mapping
VRAM_ID2	UMA/DIS type detected	1	UMA
		0	DIS



ID	Description	Setting	Mapping
VRAM_ID1	Project Series	1	Odin
		0	Antman

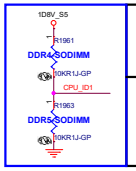


ID	Description	Setting	Mapping
AUDIO_DET	AUDIO type detected	1	ALC3254
		0	CS8409

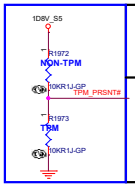


ID	Description	Setting	Mapping
NON TBT DET	NON TBT type detected	1	8010
		0	8828

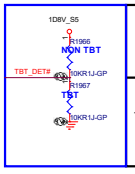
TBT R1962 stuff avoid PCH floating



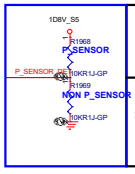
ID	Description	Setting	Mapping
DDR DET	DDR type detected	1	DDR4
		0	DDR5



ID	Description	Setting	Mapping
TPM_PRSNT#	TPM type detected	1	NON-TPM
		0	TPM



ID	Description	Setting	Mapping
TBT_DET#	TBT type detected	1	NON TBT
		0	TBT



ID	Description	Setting	Mapping
P SENSOR DET	P Sensor type detected	1	P SEN
		0	NON P

16.2.1 Configurable GPIO Voltage

Except for all pads in GPIO S, GPIO R, and GPD groups, all other GPIO groups support per-pad configurable voltage, which allows control selection of 1.8 V or 3.3 V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8 V level with 3.3 V tolerant.
- Output: the pin drives 3.3 V via a ~20 K pull-up. With this, any 1.8 V device must be capable of taking 20 K pull-up to 3.3 V.

WARNING

GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

NOTES

1. GPIO S group supports 1.8 V only.
2. GPIO R group supports per-group voltage configuration (3.3 V or 1.8 V) only.
3. GPD group supports 3.3 V only.

<Core Design>

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	019_PCH (CLK/CNVi)	
Size: Custom	Document Number: Odin ADL-P	Rev: SC
Date: Thursday, August 05, 2021	Sheet 19 of 105	

Main Func = PCH

https://vinafix.com

ESPI DEBUG
68 CPU_UART_TXD
68 CPU_UART_RXD

eDP (Touch Panel)
55,96 CPU_I2C_SDA_TS
55,96 CPU_I2C_SCL_TS

Touch Pad
55,66 CPU_I2C_SCL_TP
55,66 CPU_I2C_SDA_TP

RGB IR
55,96 CPU_I2C_SCL_IR
55,96 CPU_I2C_SDA_IR

SAR SENSOR

G-Sensor
55,70,90 CPU_I2C_SCL_GSENSOR
55,70,90 CPU_I2C_SDA_GSENSOR

55 GSEN_INT1_C
70 GSEN2_INT1_C
70 GSEN2_INT2_C
24,66 LID_CL_SIO#
24 TABLE_MODE#

55 ALS_INT
65 KB_LED_BL_DET
71,75 PCH_TBT1_PERST#
71,72 TBT_FORCE_PWR

1D8V_S0
R2002 1 10KR1J-GP ALS_INT
ANT16

ESPI DEBUG
CPU_UART_TXD
CPU_UART_RXD
GSEN_INT1_C

Touch Panel
CPU_I2C_SCL_TS
CPU_I2C_SDA_TS

E3 Touch Pad
CPU_I2C_SCL_TP
CPU_I2C_SDA_TP

Accelerometer
CPU_I2C_SCL_GSENSOR
CPU_I2C_SDA_GSENSOR

1.8V RGB IR Camara
CPU_I2C_SCL_IR
CPU_I2C_SDA_IR

CPU1F
6 OF 22
EN48 GPP_H11/UART0_TXD/IM2_SKT2_CFG1
EN46 GPP_H10/UART0_RXD/IM2_SKT2_CFG0
EL41 GPP_H13/I2C7_SCL/UART0_CTS#/M2_SKT2_CFG3/ISH_GP7B/DEVSLP1B
EK41 GPP_H12/I2C7_SDA/UART0_RTS#/M2_SKT2_CFG2/ISH_GP6B/DEVSLP0B
EW30 GPP_D18/UART1_TXD/ISH_UART1_TXD
EV34 GPP_D17/UART1_RXD/ISH_UART1_RXD
EH46 GPP_H5/I2C0_SCL
EF46 GPP_H4/I2C0_SDA
EH43 GPP_H7/I2C1_SCL
EF43 GPP_H6/I2C1_SDA
DT57 GPP_B6/ISH_I2C0_SCL/I2C2_SCL
DT56 GPP_B5/ISH_I2C0_SDA/I2C2_SDA
DR56 GPP_B8/ISH_I2C1_SCL/I2C3_SCL
DR58 GPP_B7/ISH_I2C1_SDA/I2C3_SDA
EN43 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
EL43 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD
DN60 GPP_B17/I2C5_SCL/ISH_I2C2_SCL
DN57 GPP_B16/I2C5_SDA/ISH_I2C2_SDA
ALDER-LAKE-P-GP-U1

GPP_D14/ISH_UART0_TXD/I2C4B_SCL
GPP_D13/ISH_UART0_RXD/I2C4B_SDA
GPP_D16/ISH_UART0_CTS#/I2C7B_SCL
GPP_D15/ISH_UART0_RTS#/I2C7B_SDA
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPPC_RCOMP
EY28 PCH_TBT1_PERST#
EV28 TBT_FORCE_PWR
EY36 KB_LED_BL_DET
EW36 GSEN2_INT2_C
FA34 ALS_INT
EY30 TABLE_MODE#
EY31 LID_CL_SIO#
EV31 GSEN2_INT1_C
DR61 GPPC_RCOMP 1 R2001 2 200R2F-L-GP

1.8V RGB IR Camara
ALS_INT

GPIO	GPPC_RCOMP	200 ohm +/-1% pull-down to GND	-	-	

3D3V_S0
RN2005
2 1 4 3 CPU_I2C_SCL_TS CPU_I2C_SDA_TS
SRN2K2J-1-GP
R2003 1 10KR1J-GP GSEN2_INT1_C
R2004 1 10KR1J-GP GSEN2_INT2_C
R2006 1 DX 10KR1J-GP GSEN_INT1_C

1D8V_S0
ALS_INT: ALS interrupt.
WA_DATA: I2C for ALS/ EMSA WE1
WA_CLK: I2C for ALS/ EMSA WE1
W_GPIO: EMSA WE1 interrupt.
RN2001
2 1 4 3 CPU_I2C_SCL_IR CPU_I2C_SDA_IR
ANT16
SRN2K2J-1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 020_PCH (ESPI/UART/SMB/I2C/CL/J
Size: A2
Document Number: Odin ADL-P
Rev: SC
Date: Thursday, August 05, 2021
Sheet 20 of 105

Main Func = PCH

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CNVi

61	CNV_WT_DP1
61	CNV_WT_DN1
61	CNV_WT_DP0
61	CNV_WT_DN0
61	CNV_WT_CLKP
61	CNV_WT_CLKN
61	CNV_WR_DP1
61	CNV_WR_DN1
61	CNV_WR_DP0
61	CNV_WR_DN0
61	CNV_WR_CLKP
61	CNV_WR_CLKN
61	CNV_RF_RST_N
61	CNV_BRI_RSP_PCH
61	CNV_RGI_RSP_PCH
15,61	CNV_RGI_DT_PCH
15,61	CNV_BRI_DT_PCH
61	CNV_CLKREQ

19 VRAM_ID1

CPU1J — 10 OF 22

AD41	CSI_D_DP1/CSI_C_DP2	CNV_WT_D1P	FC46 CNV_WT_DP1
AB41	CSI_D_DN1/CSI_C_DN2	CNV_WT_D1N	FA46 CNV_WT_DN1
AG41	CSI_D_DP0/CSI_C_DP3	CNV_WT_D0P	EV43 CNV_WT_DP0
AF41	CSI_D_DN0/CSI_C_DN3	CNV_WT_D0N	EY43 CNV_WT_DN0
J41	CSI_D_CLK_P	CNV_WT_CLKP	EV47 CNV_WT_CLKP
L41	CSI_D_CLK_N	CNV_WT_CLKN	EY47 CNV_WT_CLKN
P44	CSI_C_DP1	CNV_WR_D1P	EV40 CNV_WR_DP1
M44	CSI_C_DN1	CNV_WR_D1N	EY40 CNV_WR_DN1
T41	CSI_C_DP0	CNV_WR_D0P	EW42 CNV_WR_DP0
P41	CSI_C_DN0	CNV_WR_D0N	EY42 CNV_WR_DN0
J44	CSI_C_CLK_P	CNV_WR_CLKP	FA43 CNV_WR_CLKP
K44	CSI_C_CLK_N	CNV_WR_CLKN	FC43 CNV_WR_CLKN
W41	CSI_B_DP1	CNV_WT_RCOMP	FC40 CNV_WT_RCOMP
AA41	CSI_B_DN1		
C38	CSI_B_DP0	GPP_F1/CNV_BRI_RSP/UART2_RXD	EK33 CNV_BRI_RSP_PCH
A38	CSI_B_DN0	GPP_F0/CNV_BRI_DT/UART2_RTS#	EH33 CNV_BRI_DT_PCH
G39	CSI_B_CLK_P	GPP_F3/CNV_RGI_RSP/UART2_CTS#	ER31 CNV_RGI_RSP_PCH
F39	CSI_B_CLK_N	GPP_F2/CNV_RGI_DT/UART2_TXD	EN31 CNV_RGI_DT_PCH
C36	CSI_A_DP1/CSI_B_DP2	GPP_F5/MODEM_CLKREQ/CRF_XTAL_CLKREQ	EF36 CNV_CLKREQ
A36	CSI_A_DN1/CSI_B_DN2	GPP_F6/CNV_PA_BLANKING	EH36
C37	CSI_A_DP0/CSI_B_DP3	GPP_F4/CNV_RF_RESET#	ET31 CNV_RF_RST_N
E37	CSI_A_DN0/CSI_B_DN3		
F36	CSI_A_CLK_P		
G36	CSI_A_CLK_N		
A55	CSI_RCOMP#A55		
B54	CSI_RCOMP#B54		
ET41	GPP_H22/IMGCLKOUT3		
ER41	GPP_H21/IMGCLKOUT2		
EN41	GPP_H20/IMGCLKOUT1		
FA31	GPP_D4/IMGCLKOUT0/BK4/SBK4		

VRAM_ID1

ALDER-LAKE-P-GP-U1

R2102 2 1 150R2F-1-GP

R2104 1 DY 2 75KR2F-GP

R2103 1 75KR2F-GP

150R2F-1-GP 1 2 R2101 CSI_RCOMP

CAD NOTE:

R2101 RESISTOR PLACE VERY CLOSE TO RCOMP PINS
FOLLOW THE PDG GUIDELINES

PCH interface	CNV_RCOMP	150 ohm +/-1 % pull-down to GND	<0.5	-	Pkg trace + Board trace <1pF should be sufficient

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 021_PCH (SDW/HDA/ISH/GPIO)

Size: A4 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 21 of 105

Main Func = PCH

50 VCCAUX_SENSE
50 VSSAUX_SENSE
3,24,44,46,72 PROCHOT_CPU_N
40,50 VCCIN_AUX_VID0
40,50 VCCIN_AUX_VID1
97 TP_VCC_MIPILP

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CPUIN 14 OF 22

1D8V_VCCIN_AUX
3D3V_S5_PCH
1D8V_S5
VCCIN_AUX_FLTR
627205_ADL P_PDG_Rev0p8
PH/PL 100R at VR side.
1D8V_VCCIN_AUX_FLTR
Shorted on the Platform.
(200mA) 1D05V_VNN_BYPASS
(200mA) 1D05V_S5_BYPASS
VR_ALERT_N
VCCIN_AUX_VID0
VCCIN_AUX_VID1
Could be float if not use Well
ALDER-LAKE-P-GP-U1

Out Trace width need to 12mil
In (Max 135mA) Trace width need to 20mil
Out (Max 22mA) Trace width need to 12mil

Layout Note:
Motherboard routing resistance from VCC1P05_OUT_FET pin (EV3, EW1, EY1) to VCC1P05_PROC pin (EU4, EU1) should be less than 100mOhm. This value already includes the power gate resistance in order to connect both power rails.

(1.5A) Out for 1D05V_VCCST, XDP
Non-MIPI DSI

+VCCLDOSTD_0P85
Primary Side/Secondary Side (VCCLCDOSTD_0P85_A)
0D85V_S5_VCCLDOSTD_OUT
C2210 SC2D2U6D3V2MX-DL-GP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA WITHIN 2.5MM FROM PACKAGE
Table 790. Decoupling Solution

+VCCDPHY_1P24
Primary Side/Secondary Side (VCCDPHY_1P24_1)
1D24V_S5_VCCDPHY_OUT
For CNVi
C2204 SC4D7U6D3V2MX-1-GP
CAD NOTE: PLACE NEAR BGA WITHIN 5MM FROM PACKAGE
Table 786. Decoupling Solution

+VCCA_CLKLDO_1P8 (165mA)
Primary Side (VCCA_CLKLDO_1P8_1)
1D8V_S5
R2203 0R2J-2-GP
1D8V_S5_CLKLDO
C2213 SC22U6D3V2MX-1-DL-GP
C2212 SC22U6D3V2MX-1-DL-GP
CAD NOTE: Must take care this power layout and add shield GND.
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA(Pin-EB1 (Less than 18mm away.)
Table 784. Decoupling Solution

VCCPDSW_3P3 (IccMax) : 3mA
627205_ADL P_PDG_Rev0p8
3D3V_S5_PCH
C2211 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA(Pin-EB42)
Table 792. Decoupling Solution

Decap Placement	Form Factor	Value	Note
NA	NA	NA	NA

VCCPRIM_3P3 (IccMax) : 410mA
Primary Side (VCC3P3_2)
3D3V_S5_PCH
C2221 SC1U10V2KX-1DLGP
C2222 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA(Pin-EB33/EE31) (Less than 21mm away.)
Table 800. Decoupling Solution

PROCHOT_CPU_N
3D3V_S5_PCH
R2207 100KR2J-1-GP
VR_ALERT_N
D2201 RB520S30-GP
PROCHOT_CPU_N_R
PROCHOT_CPU_N
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F
R2202 0R2J-2-GP
VR_ALERT_N

+VCCIN_AUX_FIL
Primary Side (VCCIN_AUX_FILTR) (VCCIN_AUX_7)
1D8V_VCCIN_AUX_FLTR
C2220 SC22U6D3V3MX-1-GP
C2215 SC22U6D3V3MX-1-GP
C2216 SC10U6D3V2MX-2-GP

VCCDSW_1P05
Primary Side/Secondary Side (VCCDSW_1P05_2)
1D05V_DSW
C2214 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA. (Less than 15mm away.)
Table 788. Decoupling Solution

+VCC_VNNEXT_1P05V (200mA)
1D05V_VNN_BYPASS
C2201 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA.
Table 806. Decoupling Solution

Decap Placement	Form Factor	Value	Note
NA	NA	NA	NA

+VCC1P05_PROC (IccMax) : 850mA
+VCC1P05_PROC : SECONDARY (BSC)
1D05V_VCCST
C2250 SC10U6D3V2MX-2-GP
+VCC1P05_PROC : PRIMARY (TSC)
1D05V_VCCST
C2217 SC2D2U6D3V3DLGP
C2218
C2219 SC1U10V2KX-1DLGP
Follow CRB
CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO THE BGA PINS.
Table 768. Decoupling Solution

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary Side	0402	1uF	2	Place as close to the pins as possible	VCC1P05_3

+VCC1P05_OUT_PCH
1D05V_S5_VCCPRIM_OUT
C2203 SC1U10V2KX-1DLGP
Table 796. Decoupling Solution

Decap Placement	Form Factor	Value	Note
NA	NA	NA	NA

+VCC_V1P05EXT_1P05V (200mA)
1D05V_S5_BYPASS
C2202 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA.
Table 804. Decoupling Solution

Decap Placement	Form Factor	Value	Note
NA	NA	NA	NA

+VCCRTC (IccMax) : 372u
Primary Side (RTC_1)
RTC_AUX_S5
C2205 SC1U10V2KX-1DLGP
C2206 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA. (Less than 21mm away.)
Table 802. Decoupling Solution

+VCCPGPPR_3P3_1P8
3D3V_S5_PCH
3D3V_GPPR_S5
R2204 0R2J-2-GP
C2209 SC1U10V2KX-1DLGP
Trace width need to 10mil
Table 794. Decoupling Solution

Decap Placement	Form Factor	Value	Note
NA	NA	NA	NA

+VCCPRIM_1P8 (IccMax) : 1.972A
1D8V_S5
C2208 SC1U10V2KX-1DLGP
CAD NOTE: PLACE CAP CLOSEST CPOSSIBLE TO THE BGA.
Table 798. Decoupling Solution

Decap Placement	Form Factor	Value	Note
NA	NA	NA	NA

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 022_PCH (POWER&Cap)
Size: A2 | Document Number: Odin ADL-P | Rev: SC
Date: Thursday, August 05, 2021 | Sheet 22 of 105

Main Func = PCH

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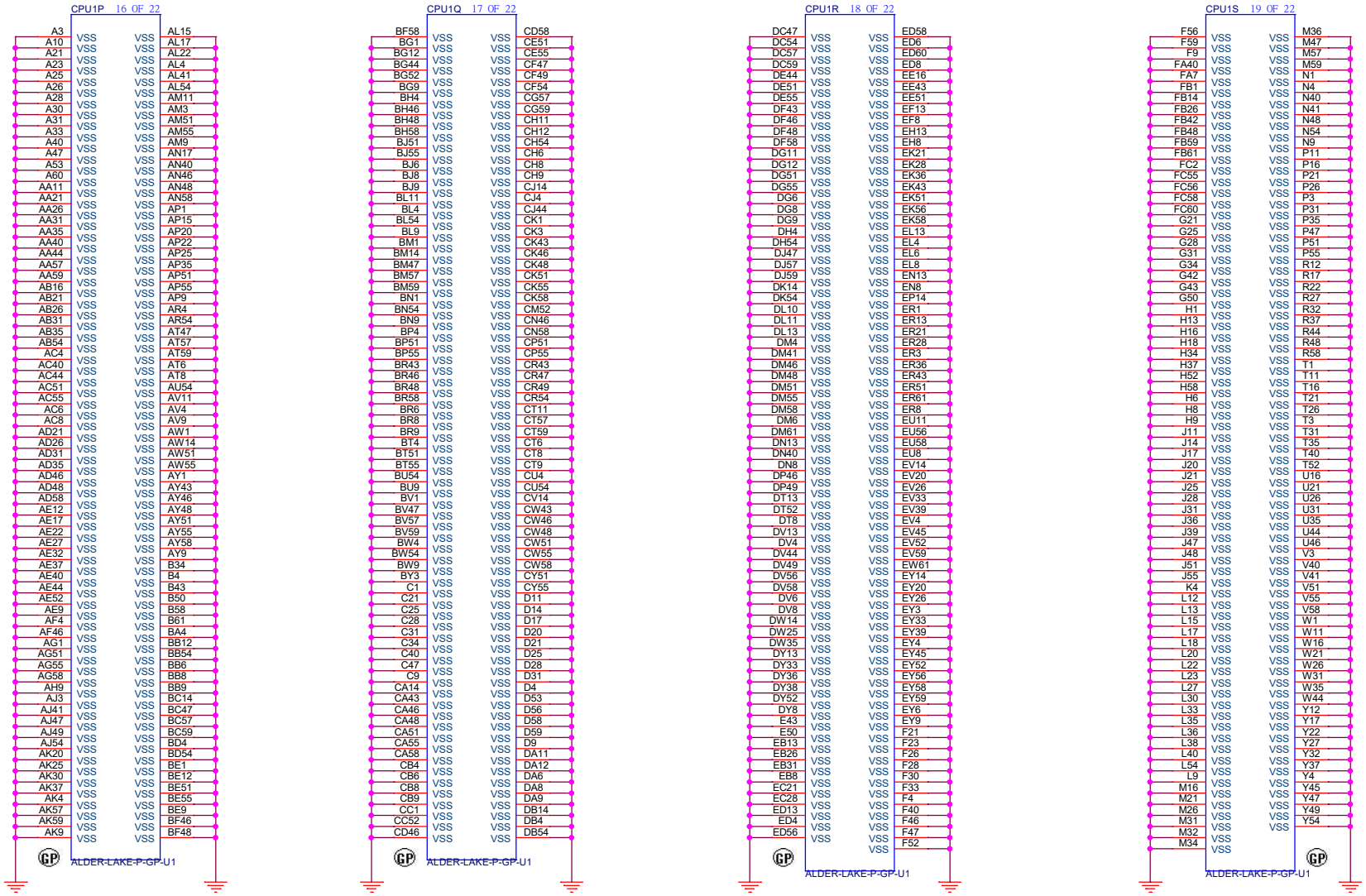

<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	023_PCH (VSS)
Size: A3	Document Number: Odin ADL-P
Rev: SC	
Date: Thursday, August 05, 2021	Sheet 23 of 105

Main Func = KBC

#	MODEL_ID(GPIO202)	PULL_LOW RESISTOR	PULL_HIGH RESISTOR	VOLTAGE
1	ODIN 14/16 N UMA	100K	10.0K	3
2	ODIN 16 V UMA	100K	17.8K	2.801
3	ANTMAN 14 UMA	100K	27.0K	2.598
4	ANTMAN 16 UMA	100K	37.4K	2.402
5	ODIN 14/16 N DIS	100K	49.9K	2.201
6	ODIN 16 V DIS	100K	64.9K	2.001
7	ANTMAN 14 DIS	100K	82.5K	1.808
8	ANTMAN 16 DIS	100K	107K	1.594
9		100K	154K	1.299
10		100K	200K	1.1

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

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For Antman 2in1

For eSPI

Layout Note: Place close to Mec1515

JTAG DEBUG CONN

BATTER / CHARGER

Antman16(TNT) R2450 stuff avoid EC floating

8010/8920 SKT

FOR ANT16

LED

PROCHOT

Power Switch Logic(PSL)

WWAN

THERMAL

SSD

SAR SENSOR

TOUCH PANEL

BL LED

FAN

CHARGE

CLOCK RESERVE

EC G3 Flash Share

For eSPI Pick one from the SPI_G3

GPIO55 (BSS_STRAP)

Already pull low on CPU side

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot Note 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/CT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI CS0# is detected high while RSMRST# is low.

R2	
R2410 R2411 R2416	
TPM	10DR 64.10005.6DL
NON TPM	49.9R 64.49R95.6DL

Wistron Corporation
KBC MEC1515
Odin ADL-P
SC

SSID = Flash.ROM

SPI FLASH ROM (32M byte) for PCH

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SPI ROM	
SHARE ROM	

18,24,68 SPI_CS_CPU_N0
18,24,68,91 SPI_SO_ROM
18,24,68 SPI_WP_ROM
18,24,68 SPI_HOLD_ROM
18,24,68,91 SPI_CLK_ROM
18,24,68,91 SPI_SI_ROM

19 RTC_DET_N
24 RTCRST_ON_POWER
24 VCCDSW_EN
17,45 3V_5V_POK

3D3V_S5_PCH
C2501 SC10U6D3V3MX-DL-GP
C2502 SCD1U16V2KX-3DLGP
R2501 4K7R2J-2-GP
U2501
CS# SO/IO1 IO2 VSS VCC IO3 SCLK SI/IO0 GND
GD25B256EYIGR-GP
SPI_SO_ROM SPI_WP_ROM
R2518 R2517 15R2J-GP 49D9R2F-GP
SPI_CS_CPU_N0 SPI_SO_ROM1 SPI_WP_ROM1
SPI_HOLD_ROM1 SPI_CLK_ROM1 SPI_SI_ROM1
R2519 R2520 R2521 49D9R2F-GP 15R2J-GP 15R2J-GP
SPI_HOLD_ROM SPI_CLK_ROM SPI_SI_ROM

072.25256.0AH1
2ND = 072.25256.0G03
3rd = 072.25673.0003
4TH = 072.25256.0AB1

Main Func = RTC

RTC GEN9

3D3V_S5
R2509 100KR2J-1-GP
VCCDSW_EN
C2505 SC1U10V2KX-1GP DY
3V_5V_POK
D2502 BAT54A-11-GP
3V_5V_PWRGD
R2510 10KR2J-3-GP

75.BAT54.07D
2ND = 75.00054.I7D
3RD = 075.00054.0Z7D

3D3V_S5
U2502 G517F1T12U-GP
EN IN OC# GND OUT
C2506 SC1U6D3V3MX-DL-GP
3D3V_S5_PCH

074.51712.009F
2ND = 074.03553.0A7F
3RD = 074.07115.009F

3D3V_RTC_AUX
Q2501 PJA3413-1-GP

084.03413.0031
2nd = 084.02301.0031
3rd = 84.03327.031

RTC_AUX_S5
R2514 4K7R2J-2-GP
RTC_3P3_EN_D
Q2502 2N7002K-2-GP-U

84.2N702.J31

RTCRST_ON_POWER
R2512 1MR2J-1-GP
RTC_3P3_EN_G
R2513 100KR2J-1-GP
C2504 SCD022U16V2KX-3DLGP

Coin battery from IOBD

3D3V_RTC_VCC
BATT_RTC
R2515 0R2J-2-GP
Internal_RTC
R2511 0R2J-2-GP
External_RTC
BATT_RTC_R
D2503 RB520S30-GP

83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

3D3V_AUX_S5
0R2J-2-GP R2505
3D3V_RTC_SYS
D2501 RB520S30-GP
R2503 47KR2F-GP DY

83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

3D3V_RTC_AUX
C2503 SC1U10V2KX-1DLGP

3D3V_S5
R2541 100KR2J-1-GP
Q2505 2N7002K-2-GP-U
RTC_DET_N
R2504 10MR2J-L-GP

84.2N702.J31

For Battery inside RTC LDO without Coin RTC
RTC_DET_N and PBAT_PRES# can combine to one NET.
Below follow KBC vendor:
To PCH: RTC_DET_N pull up 3D3V_S5_PCH
To EC: RTC_DET_N pull up 3D3V_S5
Should add a diode at PCH (D2001)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: Custom
Document Number: Odin ADL-P
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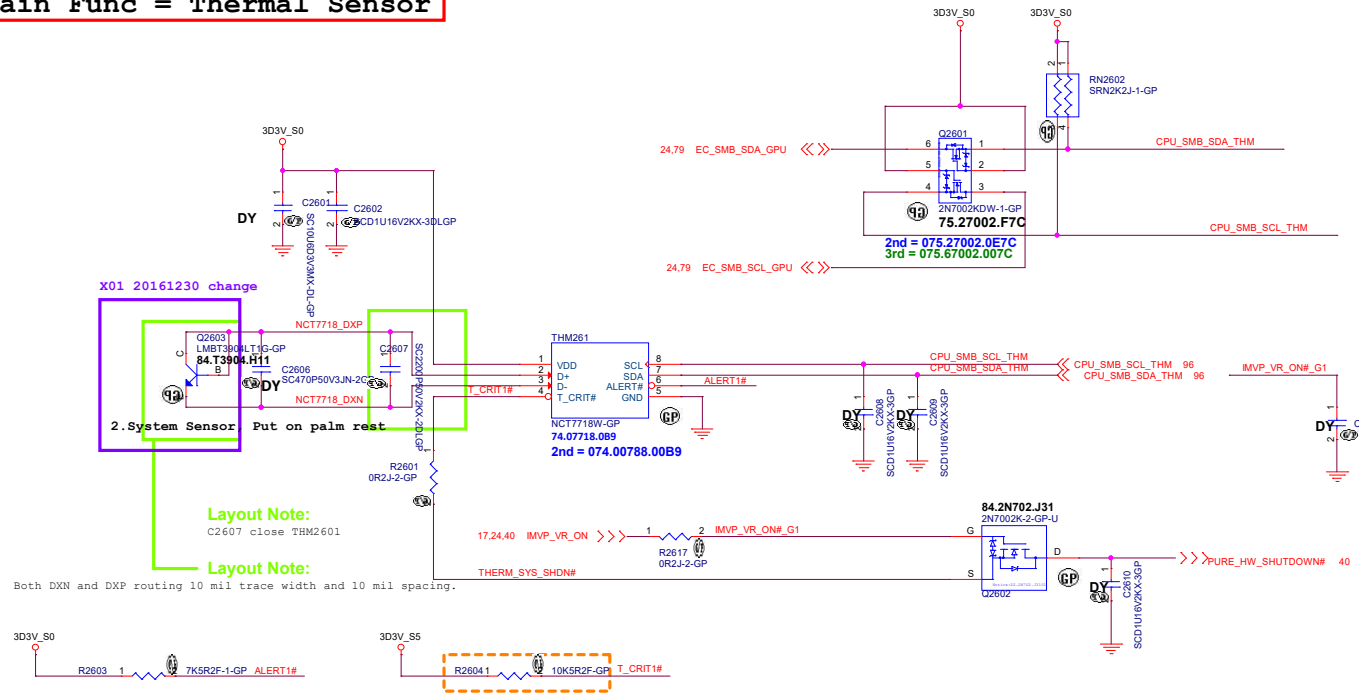
Date: Thursday, August 05, 2021
Sheet: 25 of 105

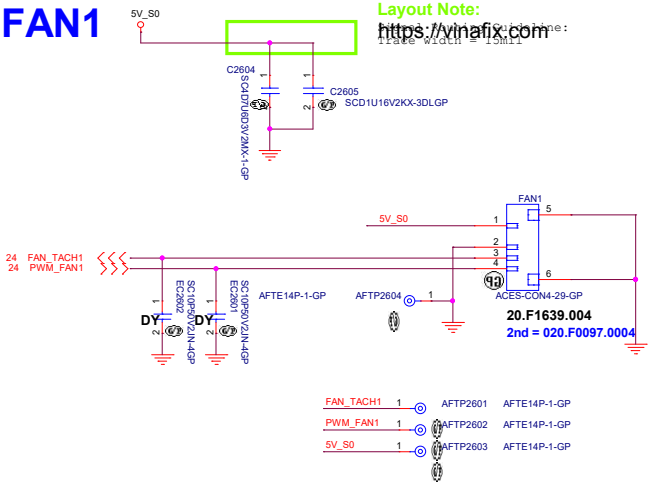
Main Func = Thermal Sensor



T_CRIT# ;ALERT# :Open-drain output pin with 12 mA sink capability

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



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<Core Design>

Wistron Corporation
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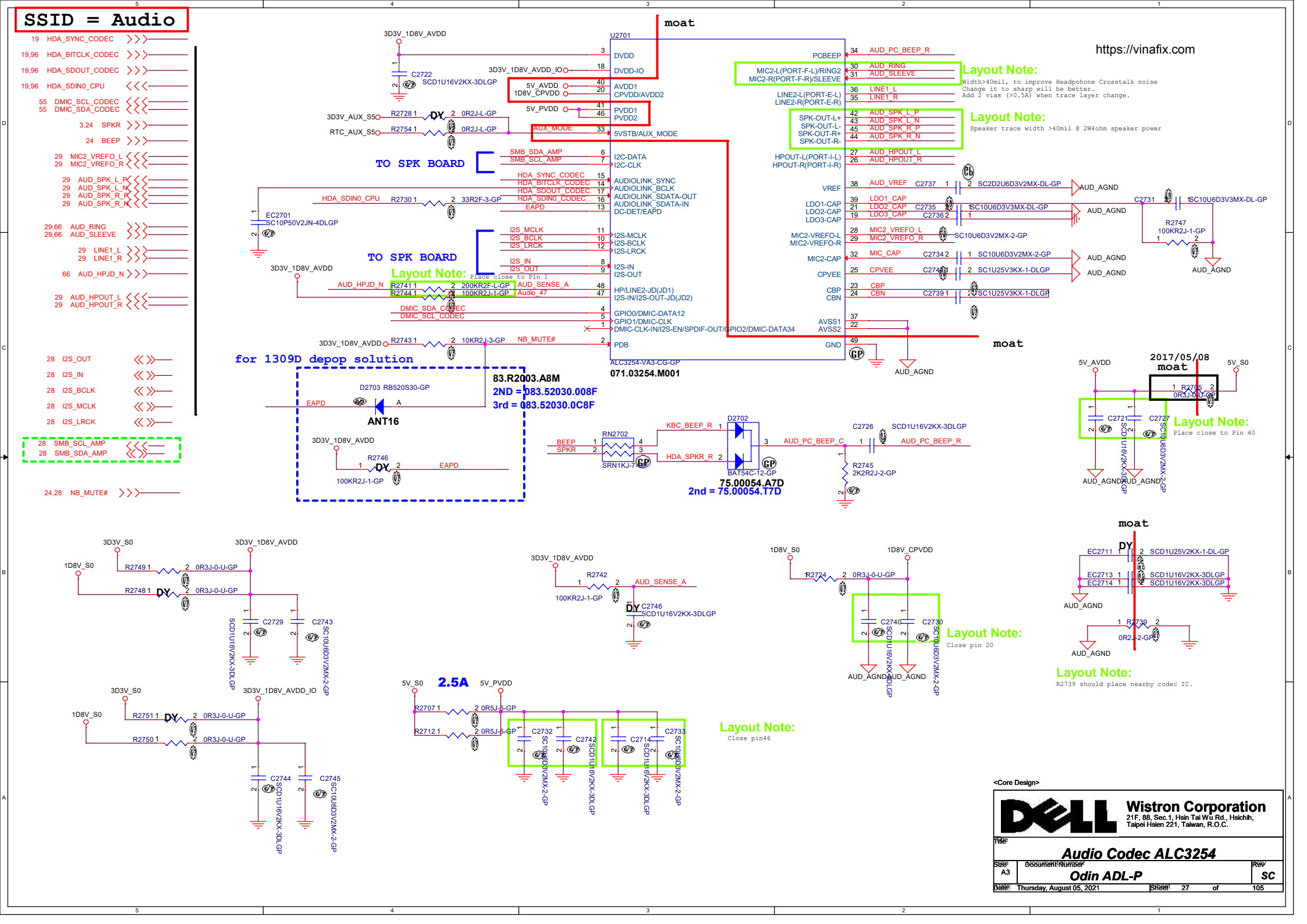
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Thermal/Fan)

Size: Custom | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 26 of 105


SSID = Audio
19 HDA_SYNC_CODEC
19,96 HDA_BITCLK_CODEC
19,96 HDA_SDOUT_CODEC
19,96 HDA_SDIN0_CPU
55 DMIC_SCL_CODEC
55 DMIC_SDA_CODEC
3,24 SPKR
24 BEEP
29 MIC2_VREFO_L
29 MIC2_VREFO_R
29 AUD_SPK_L_P
29 AUD_SPK_L_N
29 AUD_SPK_R_P
29 AUD_SPK_R_N
29,66 AUD_RING
29,66 AUD_SLEEVE
29 LINE1_L
29 LINE1_R
66 AUD_HPJD_N
29 AUD_HPOUT_L
29 AUD_HPOUT_R
28 I2S_OUT
28 I2S_IN
28 I2S_BCLK
28 I2S_MCLK
28 I2S_LRCK
28 SMB_SCL_AMP
28 SMB_SDA_AMP
24,28 NB_MUTE#
moat
U2701
ALC3254-VA3-CG-GP
071.03254.M001
TO SPK BOARD
TO SPK BOARD
Layout Note:
Place close to Pin 1
for 1309D depop solution
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F
ANT16
D2703 RB520S30-GP
BAT54C-12-GP
75.00054.A7D
2nd = 75.00054.T7D
RN2702
SRN1KJ-7-GP
Layout Note:
Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power
https://vinafix.com
2017/05/08
moat
Layout Note:
Place close to Pin 40
2.5A
Layout Note:
Close pin46
Layout Note:
Close pin 20
Layout Note:
R2739 should place nearby codec IC.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec ALC3254
Odin ADL-P
SC
Thursday, August 05, 2021
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Main Func = Audio.AMP

For Antman16
https://vinafix.com

19 SPK_ID3

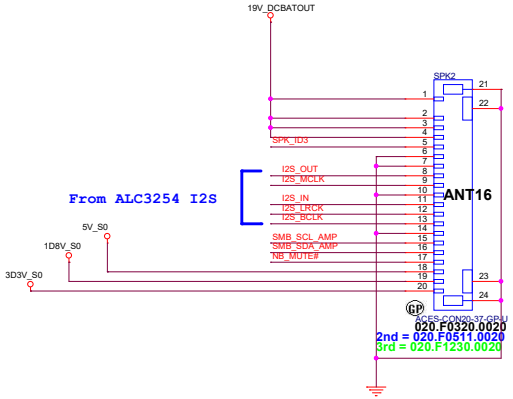
need connect to EC For BEEP Function

27 SMB_SCL_AMP
27 SMB_SDA_AMP

27 I2S_OUT
27 I2S_IN
27 I2S_BCLK
27 I2S_MCLK
27 I2S_LRCK

27,29 AUD_SPK_L_P
27,29 AUD_SPK_L_N
27,29 AUD_SPK_R_P
27,29 AUD_SPK_R_N

24,27 NB_MUTE#



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 028_Audio (Audio AMP)

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 28 of 105

Main Func = Audio

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Mainboard	Main board Pin define
pin1	SPK_R+
pin2	SPK_R-
pin3	SPK_L-
pin4	SPK_L+
pin5	SPK_DET1
pin6	GND
pin7	SPK_DET2
pin8	GND

27 AUD_SPK_L_P
27 AUD_SPK_L_N
27 AUD_SPK_R_P
27 AUD_SPK_R_N

27 MIC2_VREFO_R
27 MIC2_VREFO_L
27,66 AUD_RING
27 AUD_HPOUT_L
27 LINE1_L
27 AUD_HPOUT_R
27 LINE1_R
27,66 AUD_SLEEVE

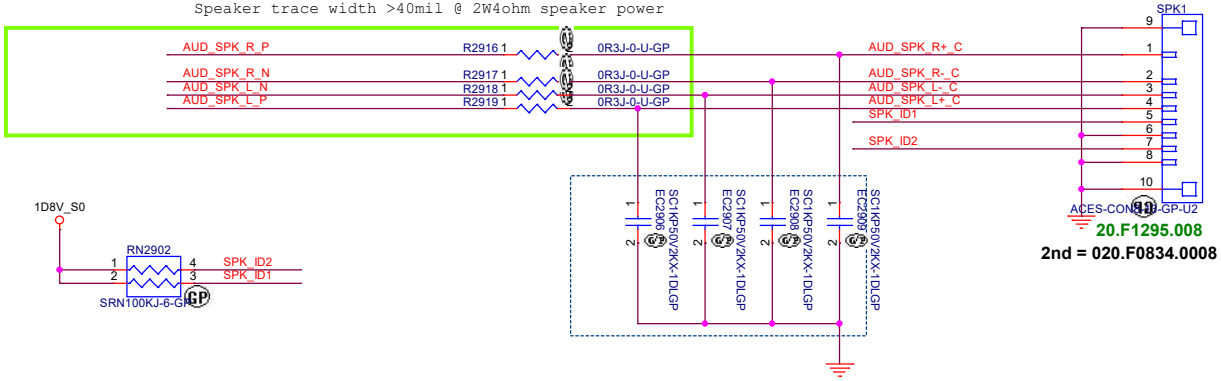
19 SPK_ID1
19 SPK_ID2

66 AUD_HP1_JACK_L1

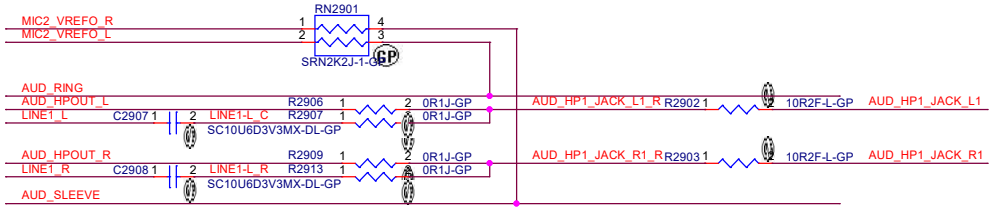
66 AUD_HP1_JACK_R1

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



Universal Jack (Moved to I/O Board)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3
Document Number: Odin ADL-P
Rev: SC
Date: Thursday, August 05, 2021
Sheet 29 of 105

https://vinafix.com

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 30 of 105

Main Func = LAN

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN RTL8106*

Size	Document Number	Rev
Custom	*Odin ADL-P*	*SC*

Date: Thursday, August 05, 2021 Sheet 31 of 105

Main Func = LAN

https://vinafix.com

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *XFOM&RJ45*

Size: A3 | Document Number: *Odin ADL-P* | Rev: *SC*

Date: Thursday, August 05, 2021 | Sheet 32 of 105

Main Func = Card Reader

https://vinafix.com

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5170

Size	Document Number	Rev
A4	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 33 of 105

Main Func = USB2.0

https://vinafix.com

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB2.0 CONN

Size | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 34 of 105

Main Func = USB3.0 Port1

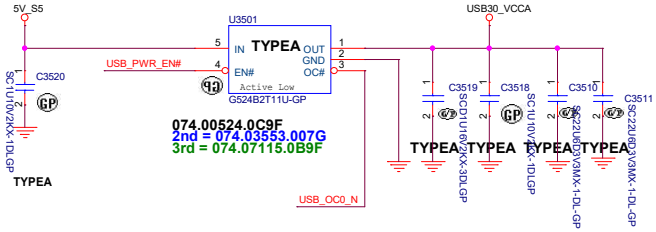
https://vinafix.com

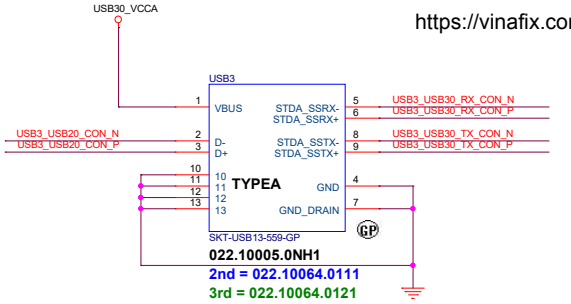
24,66 USB_PWR_EN#

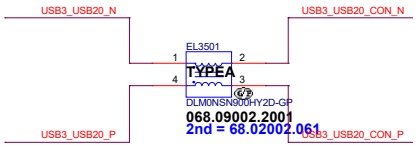
16 USB_OC0_N

16 USB3_USB20_P
16 USB3_USB20_N

16 USB3_USB30_TX_N
16 USB3_USB30_TX_P
16 USB3_USB30_RX_N
16 USB3_USB30_RX_P

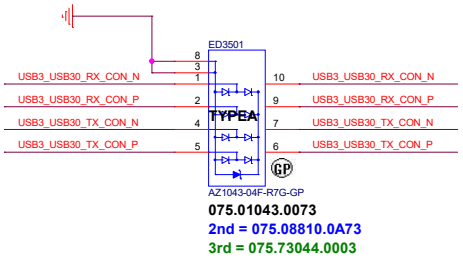


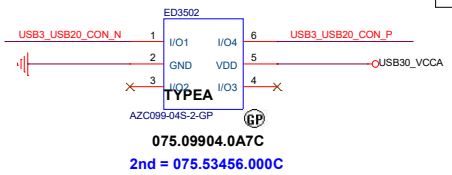


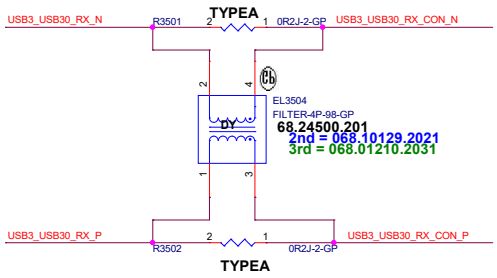


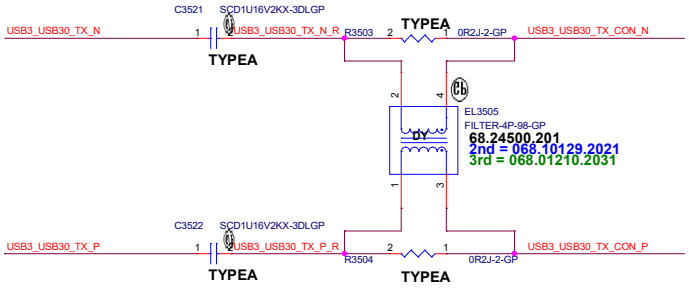
USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	









<Core Design>

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Title: USB3.0 CONN

Size	Document Number	Rev
Custom	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 35 of 105

Main Func = USB Charger

https://vinafix.com

<Core Design>

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Title: *USB Charger*

Size	Document Number	Rev
Custom	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 36 of 105

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(Blanking)

<Core Design>

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Title: USB3.0 PORT

Size	Document Number	Rev
A4	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 37 of 105

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Title

Reserved

Size	Document Number	Rev
A4	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 38 of 105

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Title

(RSVD)

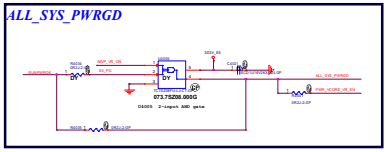
Size	Document Number	Rev
A4	***Odin ADL-P***	***SC***

Date: Thursday, August 05, 2021 Sheet 39 of 105

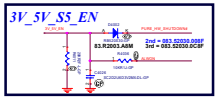
Main Func = Platform.Sequence

RUNPWROK

ALL_SYS_PWRGD

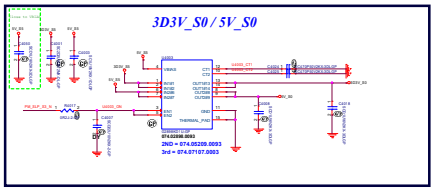


3V_5V_S5_EN

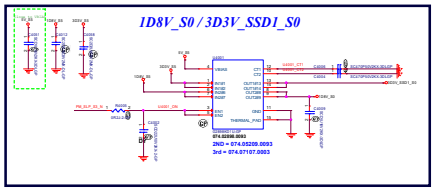


https://vinafix.com

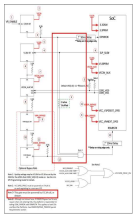
3D3V_S0 / 5V_S0



1D8V_S0 / 3D3V_SSD1_S0

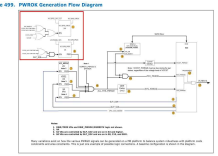


1D05V_BP_PWRGD



PWR_1D8V_CPU_EN

Figure 499. PWROK Generation Flow Diagram



VCC_V1P05EXT_1P05 / VCC_VNNEXT_1P05

Stradale MLK EVT(20200805)
(1)BYPASS STUFF, except R4039 R4030 PR5431 PR5432 PR5402 are DY.
(2)NON BYPASS DY, except R4032 is stuff.

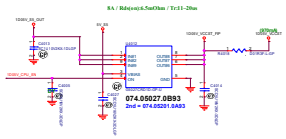
PWM_1D05V_EN use the RC delay.

Stradale MLK EVT(20200805)
(1)BYPASS for Premium
(2)NON BYPASS for Volume

Page 54 PG pin reserve bayppass RES.

627205_ADL_P_PDG_RevUp01

1D05V_VCCST



Note 2: VCC1P05_PROC must be powered on if AUX is on and regulating to a non-zero VID

V1.05U_CPU GENERATION

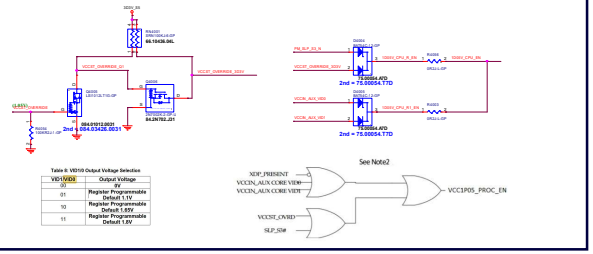


Table 8: VID10 Output Voltage Selection

VID10 (VID[9])	Output Voltage
01	Register Programmable Default 1.1V
10	Register Programmable Default 1.05V
11	Register Programmable Default 1.0V

See Note2

XDP_PRESENT
VCCIN_AUX_CORE VID[9]
VCCIN_AUX_CORE VID[9]
VCCST_OVRD
SLP_S3#

VCC1P05_PROC_EN

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640_Sequence (Power on)

Project: Odin ADL-P
Size: B
Rev: SC

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<Core Design>

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Title
Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	*Odin ADL-P*	*SC*

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A4	Odin ADL-P	SC

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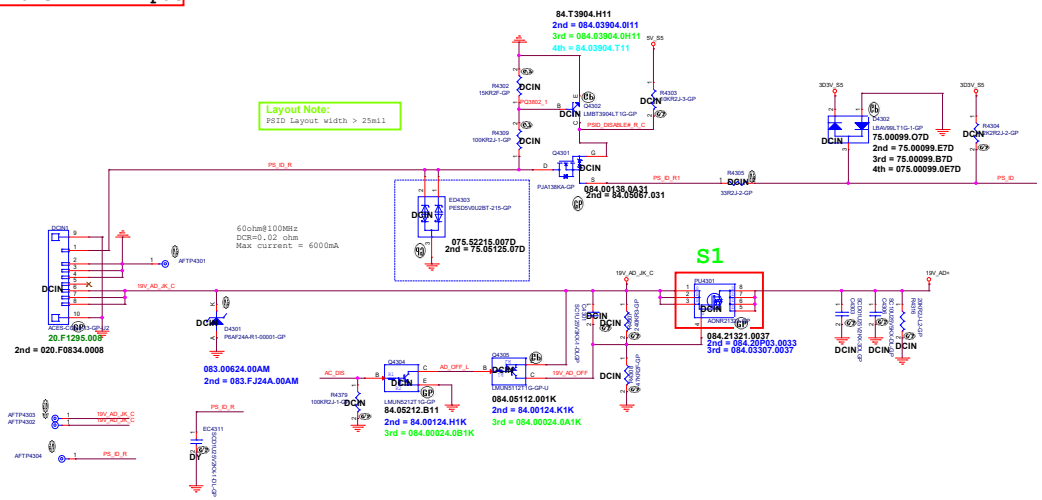
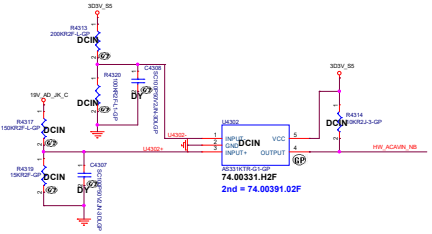
24.44 AC_DIS
24 PS_ID
24.44 HW_ACAVIN_NB
44.89 19V_AD_JK_C
24.44,96 PBAT_CHG_SMBCLK
24.44,96 PBAT_CHG_SMBDAT
24.44,66 PBAT_PRES#

SIV Auto Test

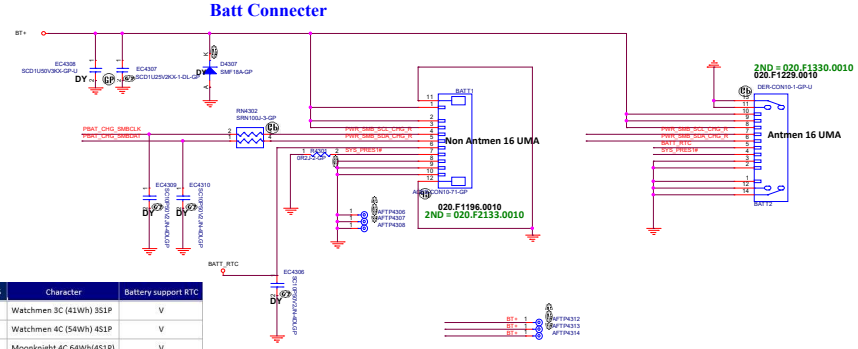
Main Func = ADT Input



Barrel Adapter Piug-in Detect



Main Func = M-BAT Input



N14	N16	V16	Antman 14	Antman 16	Character	Battery support RTC
		v	v		Watchmen 3C (41Wh) 3S1P	V
v	v	v	v		Watchmen 4C (54Wh) 4S1P	V
v	v			v	Moonknight 4C 64Wh(4S1P)	V
				v	Horizon 6C(87Wh) 3S2P	V

<Core Design>
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
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Title: DCIN
Size: A1
Document Number: Odin ADL-P
Rev: SC
Date: Thursday, August 05, 2021
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ISL9538C For Charger

https://vinafix.com

Main Func = Charger

OFFPAGE

EE needs check it!!

I2C form EC

To EC

ISL9538 AMON/BMON to EC

From NXP ACK

E3

S2

074.09538.M001
2nd = 074.09538.0C73

DCR=8mm~9m Ohm,
Idc=13A, Isat=16A
10.0mm x 11.5mm x 3.0mm

PR4413 change to 11.5K (64.11525.6DL) for Athena

0523

PU 3V3_AON_S0 on GPU side

OPS

PU +VCCSTG = 1.0 V on CPU side

75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C

TypeC Prochot
Follow custormer circuits.

CHECK EE
follow custormer circuits.

+3D3V_VDD_DCIN

Only L

Vcore_OVP

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)						
MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIm/aL Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

Only for L	Location
L	D8604
L	PC44A9
L	PC44C2
L	PC44C3
L	PD44A2
L	PD44A3
L	PD44A4
L	PD44C1
L	PQ4423
L	PR44A0
L	PR44A1
L	PR44A4
L	PR44A7
L	PR44C1
L	PR44C2
L	PR44C3
L	PR44C4
L	PR44C7
L	PR4455
L	PR4456
L	PR4457
L	PR4493
L	PU44C1
DY	PC44C1
DY	PC4458
DY	PR44A8
DY	PR4496

INTEL CONFIDENTIAL

Wistron Corporation
Power (Charger_ISL9538)
Odin ADL-P
Thursday, August 26, 2021

OFFPAGE-Signal

40,45 3V_5V_EN — PG4559 — PWR_5V_EN

0R0402-PAD

PH on EE Side

17,25,45 3V_5V_POK — PG4560 — PWR_5V_PG

0R0402-PAD

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_5V

PG4514 GAP-CLOSE-PWR-3-GP

PG4515 GAP-CLOSE-PWR-3-GP

PG4517 GAP-CLOSE-PWR-3-GP

PG4519 GAP-CLOSE-PWR-3-GP

PG4521 GAP-CLOSE-PWR-3-GP

PG4523 GAP-CLOSE-PWR-3-GP

5V_S5 — PWR_5V

PG4506 GAP-CLOSE-PWR-3-GP

PG4507 GAP-CLOSE-PWR-3-GP

PG4513 GAP-CLOSE-PWR-3-GP

PG4508 GAP-CLOSE-PWR-3-GP

PG4509 GAP-CLOSE-PWR-3-GP

PG4516 GAP-CLOSE-PWR-3-GP

PG4510 GAP-CLOSE-PWR-3-GP

5V_AUX_S5 — PWR_5V_LDO

PG4527 GAP-CLOSE-PWR-3-GP

SY8288C For 5V

https://vinafix.com

PWR_DCBATOUT_5V

PD4502 AZ4024-01L-R7G-GP

083.04024.0AA1

2nd = 83.PJSD2.0AF

5V_AUX_S5

DY PR4552 100KR2J-1-GP

PWR_DCBATOUT_5V

PC4552 SCD1U25V2KX-1DL-GP

PC4554 SC10U25V6KX-DL-GP

PU4551

IN#2 IN#3 IN#4 IN#5

NC#10 NC#16 VCC EN1 EN2

PG BS LX#6 LX#19 LX#20 OUT FF LDO

GND GND GND GND

PWR_5V_PG PWR_5V_BOOT PWR_5V_PH PWR_5V_VOUT PWR_5V_FB PWR_5V_LDO

PWR_5V_VCC PWR_5V_EN PWR_5V_EN2

PC4562 SC4D7U6D3V2MX-1-GP

PR4556 1MR2J-1-GP

PR4557 499KR2F-1-GP

PR4558 499KR2F-1-GP

SCD1U25V2KX-1-DL-GP

DY PC4564

SY8288CRAC-GP

074.08288.0B43

2ND = 074.05068.0043

PC4553 SCD1U25V2KX-1-DL-GP

Cyntec. 6.8 x7.3 x 3.0mm

DCR: 14~15mOhm

Idc : 9A , Isat : 18A

PL4551

IND-1D5UH-23-GP-U

68.1R510.10K

2ND = 68.1R51A.10F

Design Current=8A

Trace used 10 mil

PG4562 GAP-CLOSE-PWR-3-GP

PWR_5V_FB_A

PC4563 SC1K50V2KX-1DLGP

PR4555 1KR2F-3-GP

PWR_5V

DY PC4565 PC4556 PC4557 PC4558 PC4559 PC4560 DY PC4561

SCD1U25V2KX-1-DL-GP

SC22U6D3V3MX-1-DL-GP

PC4551 SC10U6D3V3MX-DL-GP

OFFPAGE-Signal

40,45 3V_5V_EN — PG4561 — PWR_3D3V_EN

0R0402-PAD

PH on EE Side

17,25,45 3V_5V_POK — PG4563 — PWR_3D3V_PG

0R0402-PAD

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_3D3V

PG4501 GAP-CLOSE-PWR-3-GP

PG4502 GAP-CLOSE-PWR-3-GP

PG4503 GAP-CLOSE-PWR-3-GP

PG4505 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_3D3V

PG4504 GAP-CLOSE-PWR-3-GP

PG4520 GAP-CLOSE-PWR-3-GP

PG4522 GAP-CLOSE-PWR-3-GP

PG4528 GAP-CLOSE-PWR-3-GP

PG4524 GAP-CLOSE-PWR-3-GP

PG4526 GAP-CLOSE-PWR-3-GP

PG4529 GAP-CLOSE-PWR-3-GP

PG4525 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PWR_3D3V_LDO

PG4512 GAP-CLOSE-PWR-3-GP

SY8288B For 3D3V

PWR_DCBATOUT_3D3V

PD4501 AZ4024-01L-R7G-GP

083.04024.0AA1

2nd = 83.PJSD2.0AF

Vin Operating range : 4~23V

Vin_Max : 25V

Ilimt : 8A

PWR_DCBATOUT_3D3V

PC4501 SCD1U25V2KX-1-DL-GP

PC4502 SC10U25V6KX-DL-GP

PC4503 SC10U25V6KX-DL-GP

PU4502

IN#2 IN#3 IN#4 IN#5

NC#10 NC#15 NC#16 EN1 EN2

BS PG FF OUT LDO

GND GND GND GND

LX#6 LX#19 LX#20

PWR_3D3V_EN PWR_3D3V_EN2 PWR_3D3V_BOOT PWR_3D3V_PG PWR_3D3V_FB PWR_3D3V_PH PWR_3D3V_LDO

PR4514 1MR2J-1-GP

SY8288BRAC-GP

074.08288.0A43

2ND = 074.05168.0043

PWR_3D3V_BOOT PR4501 0R0402-PAD-1-GP PWR_3D3V_BOOT_A

PC4506 SCD1U25V2KX-1-DL-GP

Cyntec. 6.8 x7.3 x 3.0mm

DCR: 14~15mOhm

Idc : 9A , Isat : 18A

PL4501

IND-1D5UH-23-GP-U

68.1R510.10K

2ND = 68.1R51A.10F

Design Current=8A

PWR_3D3V

DY PC4513 PC4509 PC4510 PC4511 DY PC4512

SCD1U25V2KX-1-DL-GP

SC22U6D3V3MX-1-DL-GP

PWR_3D3V_LDO

PC4507 SC10U6D3V3MX-DL-GP

Trace used 10 mil

PWR_3D3V_VOUT

PG4530 GAP-CLOSE-PWR-3-GP

PC4526 SC1KP50V2KX-1DLGP

PWR_3D3V_FB2

PR4506 1KR2F-3-GP

19V_DCBATOUT

PR4509 499KR2F-1-GP

PR4508 499KR2F-1-GP

DY PC4508 SCD1U25V2KX-1-DL-GP

DY PR4505 100KR2J-1-GP

3D3V_AUX_S5

<Core Design>

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8270C & SY8388B3_5V/3D3V

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 45 of 105

Main Func = CPU.CorePower

OFFPAGE

40,97 PWR_VCORE_VR_EN — PR4619 1 0R1J-GP — PWR_VCCIN_EN

17 PWR_VCORE_VR_READY — PR4617 1 0R1J-GP — PWR_VCCIN_VRRDY

3,22,24,44,72 PROCHOT_CPU_N — PR4614 1 75R1F-GP — PWR_VCCIN_VRHOT#

44 CHGR_PSYS_IMVP — PR4652 1 0R1J-GP — PWR_VCCIN_PSYS

VCCIN PWM
47 PWR_VCCCORE_PWM1
47 PWR_VCCCORE_PWM2

VCCGT PWM
48 PWR_VCCGT_PWM8

VCCIN CS
47 PWR_VCCCORE_CS1
47 PWR_VCCCORE_CS2

VCCGT CS
48 PWR_VCCGT_CS8

47,48 PWR_VCCIN_VTEMP
47 PWR_VCCCORE_SYNC
48 PWR_VCCGT_SYNC
50 PWR_VCCAUX_IMON_A

VCCCORE SENSE
7 VCCCORE_SENSE
7 VSSCORE_SENSE

VCCGT SENSE
8 VCCGT_SENSE
8 VSSGT_SENSE

SMBUS
TP4601 PWR_VCCIN_SCL_P
TP4602 PWR_VCCIN_SDA_P

SVID
PWR_CORE_VCCST
PR4618 100R1F-GP, PR4636 100R1F-GP, PR4605 45D3R1F-GP, PC4606 SC0U1I16V2KX-3DLGP
97 SVID_CLK_CPU — 0R2J-2-GP PR4630 — PWR_VCCIN_SCLK
7 SVID_ALERT_CPU_N — 0R2J-2-GP PR4634 — PWR_VCCIN_ALT#
7 SVID_DATA_CPU — 0R2J-2-GP PR4602 — PWR_VCCIN_SDIO

VCCCORE SENSE 1D6V_CPU_CORE
PH/PL at EE Side.
PR4638 100R1F-GP
VCCCORE_SENSE — PR4628 1 0R1J-GP — PWR_VCCIN_VOSENA
VSSCORE_SENSE — PR4637 1 0R1J-GP — PWR_VCCIN_VORTNA
PR4639 100R1F-GP

VCCGT SENSE 1D52V_VCCGT
PH/PL at EE Side.
PR4642 100R1F-GP
VCCGT_SENSE — PR4640 1 0R1J-GP — PWR_VCCIN_VOSENB
VSSGT_SENSE — PR4641 1 0R1J-GP — PWR_VCCIN_VORTNB
PR4643 100R1F-GP

EE side Link
SVID Pull High V
1D05V_VCCST — PG4601 GAP-CLOSE-PWR-3-GP — PWR_CORE_VCCST

CHECK EE

PULL HIGH AT EE SIDE
3D3V_S5
PR4632 DY 10KR1J-GP PWR_VCCIN_SCL_P
PR4644 DY 10KR1J-GP PWR_VCCIN_SDA_P
PR4645 DY 10KR1J-GP PWR_VCCIN_VRRDY
PR4646 DY 10KR1J-GP PWR_VCCIN_EN
PWR_CORE_VCCST
PR4647 DY 10KR1J-GP PWR_VCCIN_VRHOT#

PR4610 1K13R2F-1-GP 18W
PR4607 909R2F-GP 28W
PC4616 SC1U25V2KX-4-GP DY
PWR_VCCIN_VFBA_C — PR4650 DY 10KR2F-2-GP
PC4617 SC1U25V2KX-4-GP DY
PWR_VCCIN_VFBB_C — PR4651 DY 10KR2F-2-GP
PR4613 1K27R2F-L-GP — PWR_VCCIN_VDIFFB

PWR_VCCIN_VDD18
PR4602 1KR2F-3-GP — PWR_VCCIN_CSSUMA
PR4634 DY 0R1J-GP
PR4629 1KR2F-3-GP — PWR_VCCIN_CSSUMB
PR4612 DY 0R1J-GP
19V_DCBATOUT
PR4601 2MR1F-GP
PR4624 133KR1F-GP
PC4607 SCD1U25V2KX-1-DL-GP

PU4601 MP2964GQKT-1503-Z-GP
074.02964.M007
CPUCore/OPT

12	VDIFFB	CS1	7
11	VORTNA	CS2	6
10	VOSENA	CS3	5
9	VFBA	CS4	4
8	VDIFFA	NC#3	3
13	VFBB	NC#2	2
14	VOSENB	NC#1	1
15	VORTNB	CS5	48
16	CSSUMA	CS6	47
17	CSSUMB	VIN_SEN	46
18	IMONA	PSYS	45
19	IMONB	TEMP	44
20	AUX_IMON	VDD33	43
21	VDD18	PWM1	42
22	SCLK	PWM2	41
23	SDIO	PWM3	40
24	ALT#	PWM4	39
49_THM	THERMAL_PAD	ADDR	38
		NC#37	37
25	VRRDY	PWM6	34
26	VRHOT#	PWM5	35
27	SDA_P	NC#36	36
28	SCL_P		
29	VID_STRAP		
30	STBB		
31	STBA		
32	PE		
33	EN		

PWR_VCCIN_VDD18
PR4609 4D7R3F-L-GP
3D3V_S5
PC4601 SC4D7U6D3V2MX-1-GP
PWR_VCCIN_ADDR
PR4655 DY 0R2F-1-GP
PR4654 0R2F-1-GP

PC4618 SC47P50V2KX-3DLGP
PC4615 SC47P50V2KX-3DLGP
PR4615 7K15R2B-GP
PC4603 SC1U25V3KX-1-DLGP
PWR_VCCAUX_IMON_R
PR4604 124R2F-U-GP

PWR_VCCIN_VRRDY
PWR_VCCIN_VRHOT#
PWR_VCCIN_SDA_P
PWR_VCCIN_SCL_P
PWR_VCCIN_VIDSTRAP
PWR_VCCGT_PWM8
PWR_VCCIN_EN
PWR_VCCIN_PE
PWR_VCCGT_SYNC
PWR_VCCCORE_SYNC
PR4635 DY 0R2J-2-GP

for ADL 28W 074.02964.M028
for ADL 15W 074.02964.M029

PSYS
PR4620 DY 0R2J-2-GP
PWR_VCCIN_PSYS
PC4604 SC330P50V2KX-3-DL-GP

TEMP
PWR_VCCIN_VTEMP
PC4608 SC1U25V3KX-1-DLGP
PR4631 49K9R1F-GP

PE
3D3V_S5
PR4622 DY 10KR2F-2-GP
PWR_VCCIN_PE
PC4612 DY SC1U25V2KX-1-DL-GP
PR4649 0R2J-2-GP

STRAP
3D3V_S5
PR4626 10KR2F-2-GP
PWR_VCCIN_VIDSTRAP
PC4602 DY SCD1U25V2KX-1-DL-GP
PR4648 DY 0KR2F-3-GP

IMONA
PR4611 36KR2F-GP
PWR_VCCIN_IMONA
PR4653 13KR2F-GP 45W
PR4627 26W 2K74R2F-GP
PC4609 SC560P50V2KX-2DLGP 28W
PC4611 SC390P50V2KX-1-GP 15W

IMONB
PR4608 56K2R2F-2-GP
PWR_VCCIN_IMONB
PR4621 10K5R2F-GP
PC4610 SC330P50V2KX-3-DL-GP

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<Core Design>
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: 046_Power (MP296`_IMVP9.1(1/3))
Size: A2 | Document Number: Stradale ADL-P | Rev: SC
Date: Thursday, August 05, 2021 | Sheet 46 of 105

Main Func = CPU.CorePower

OFFPAGE

46 PWR_VCCCORE_PWM1
46 PWR_VCCCORE_PWM2

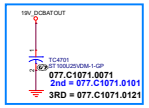
46 PWR_VCCCORE_CS1
46 PWR_VCCCORE_CS2

46 PWR_VCCCORE_SYNC
46,48 PWR_VCCIN_VTEMP

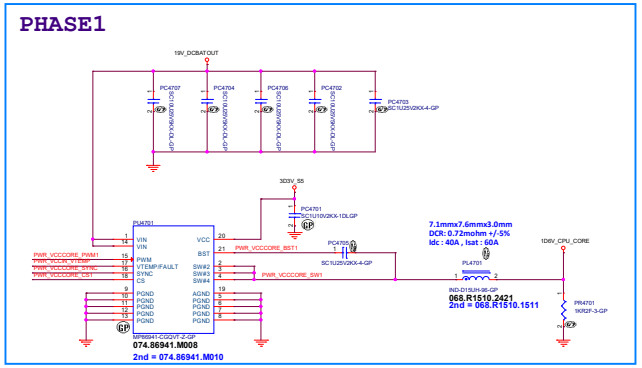
MP86971 For VCCIN

https://vinafix.com

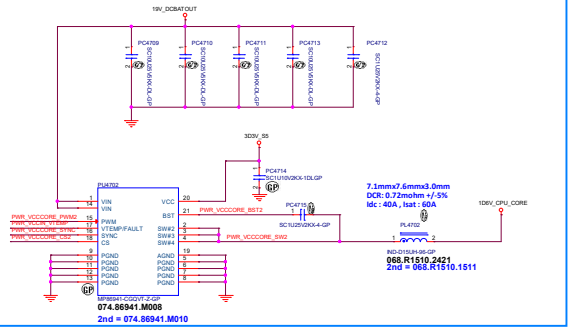
For acoustic noice



PHASE1



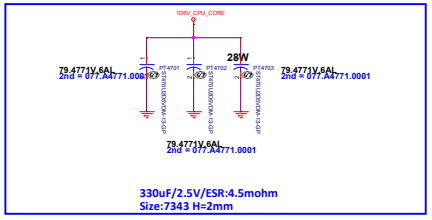
PHASE2



ADL-P U28 baseline
TDC:47A
Iccmax:80A
96A<OCP>112A

ADL-P U15 baseline
TDC:32A
Iccmax:60A
72A<OCP>84A

VCCIN Output cap



330uF/2.5V/ESR:4.5mohm
Size:7343 H=2mm

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 047_Power (MP86971_VCCIN(2/3))

Size: A3 | Document Number: Stradale ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 47 of 103

Main Func = CPU.CorePower

MP86971 For VCCGT

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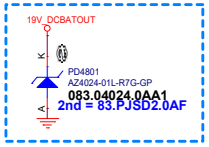
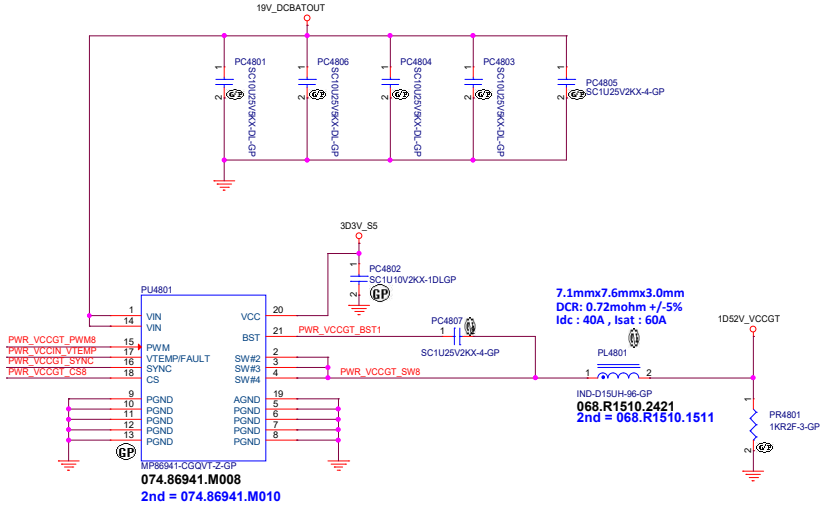
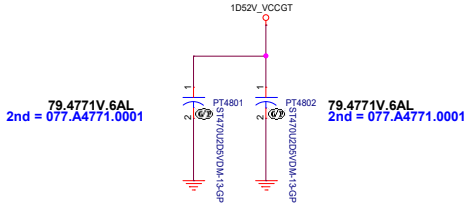
46 PWR_VCCGT_PWM8
46 PWR_VCCGT_CS8
46 PWR_VCCGT_SYNC
46,47 PWR_VCCIN_VTEMP





ADL-P U15/U28 baseline
TDC:23A
Iccmax:40A
48A<OCP>56A



330uF/2.5V/ESR:4.5mohm
Size:7343 H=2mm

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 048_Power (MP86971_VCCGT(3/3))
Size: C
Document Number: Stradale ADL-P
Rev: SC
Date: Thursday, August 05, 2021
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15W base-->2+1+1
15W per-->2+1+1
28W base-->2+1+1
28W per-->3+2+1
45W base-->3+2+1
45W per-->4+2+1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(RSVD)*

Size: A | Document Number: *Odin ADL-P* | Rev: *SC*

Date: Thursday, August 05, 2021 | Sheet 49 of 105

MP2961GL For VCCIN_AUX

https://vinafix.com

OFFPAGE

VID

VCCIN_AUX_VID0 — PR5002 0R2F-1-GP — PWR_VCCIN_AUX_VID0

VCCIN_AUX_VID1 — PR5003 0R2F-1-GP — PWR_VCCIN_AUX_VID1

PWR_1D8V_PG — PR5004 0R2F-1-GP — PWR_VCCIN_AUX_EN_R

PR5006 0R2F-1-GP

PWR_VCCIN_AUX_PG — PWR_VCCIN_AUX_PG_R

VCCIN_AUX SENSE

VCCAUX_SENSE

VSSAUX_SENSE

VCCIN_AUX IMON

PWR_VCCAUX_IMON_A — PR5017 0R2F-1-GP — PWR_VCCIN_AUX_IMON

19V_DCBATOUT — PD5001 AZ4024-01L-R7G-GP

083.04024.0AA1

2nd = 83.PJSD2.0AF

For acoustic noice

19V_DCBATOUT — TC5001 ST100U25VDM-1-GP

077.C1071.0071

2nd = 077.C1071.0101

3RD = 077.C1071.0121

ADL-P U15/U28 Baseline
TDC=14A
ICCMAX=32A
38.4A<OCP<44.8A

19V_DCBATOUT

PC5006 SC100U25V6KX-DL-GP

PC5007 SC100U25V6KX-DL-GP

PC5008 SC100U25V6KX-DL-GP

PC5013 SC100U25V6KX-DL-GP

PC5005 SC1U10V2KX-1DLGP

VCCINAUX_AGND

3D3V_S5 — PR5005 5D1R2F-GP — PWR_VCCIN_AUX_3V3

PU5001

MP2961GL-Z-GP

074.02961.M001

Pin	Name
2	VIN
18	3V3
5	VID1
6	VID0
4	IMON
7	LL
8	EN
9	PG
15	MODE1
14	MODE2
13	BST1
10	BST2
12	SW1
11	SW2
16	VOUT
17	RGND
1	PGND
3	PGND
19	AGND

PWR_VCCIN_AUX_VID1
PWR_VCCIN_AUX_VID0
PWR_VCCIN_AUX_IMON
PWR_VCCIN_AUX_LL
PWR_VCCIN_AUX_EN_R
PWR_VCCIN_AUX_PG_R
PWR_VCCIN_AUX_MODE1
PWR_VCCIN_AUX_MODE2

PR5007 7K32R2F-GP

PR5008 0R2F-1-GP

PR5009 0R2F-1-GP

PR5010 150KR2F-L-GP

PWR_VCCIN_AUX_3V3 — PR5001 100KR2F-L1-GP — PWR_VCCIN_AUX_PG_R

PR5016 0R2F-1-GP — VCCINAUX_AGND

PC5001 SCD22U25V3KX-DL-GP

PC5004 SCD22U25V3KX-DL-GP

PWR_VCCIN_AUX_BST1
PWR_VCCIN_AUX_BST2
PWR_VCCIN_AUX_PHASE
PWR_VCCIN_AUX_VOUT
PWR_VCCIN_AUX_RGND

PL5001 IND-D15UH-96-GP

068.R1510.2421

2nd = 068.R1510.1511

7.1mmx7.6mmx3.0mm
DCR: 0.72mohm +/-5%
Idc : 40A , Isat : 60A

1D8V_VCCIN_AUX

PT5001 ST470U2D5VDM-13-GP

79.4771V.6AL

2nd = 077.A4771.0001

330uF/2.5V/ESR:4.5mohm
Size:7343 H=2mm

VID0	VID1	Vout	IMON
0	0	0.00V	Disable
0	1	1.10V	Disable
1	0	1.65V	Enable
1	1	1.80V	Enable

Interleaving	VID Down	MODE1/PR5009
N	Slew down	0 ohm
Y	Slew down	90k ohm
Y	Decay	150k ohm
N	Decay	>230k ohm or float

FS	CLM	MODE2/PR5010
800kHz	12A	0 ohm
1200kHz	12A	90k ohm
800kHz	17A	150k ohm
1200kHz	17A	>230k ohm or float

Loadline	LL/PR5008
1m ohm	0 ohm
1.5m ohm	90k ohm
2m ohm	150k ohm
2.5m ohm	>230k ohm or float

VCCIN_AUX SENSE

1D8V_VCCIN_AUX

PR5011 100R2F-L1-GP-U

VCCAUX_SENSE — PR5012 0R2F-1-GP — PWR_VCCIN_AUX_VOUT

VSSAUX_SENSE — PR5013 0R2F-1-GP — PWR_VCCIN_AUX_RGND

PR5014 100R2F-L1-GP-U

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MP2961G_VCCIN_AUX

Size: C | Document Number | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 50 of 105

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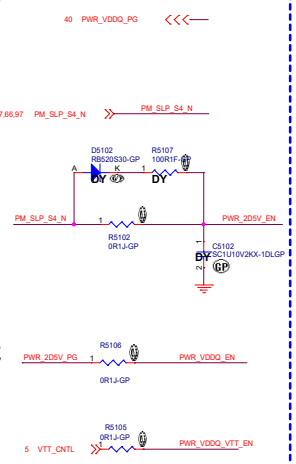
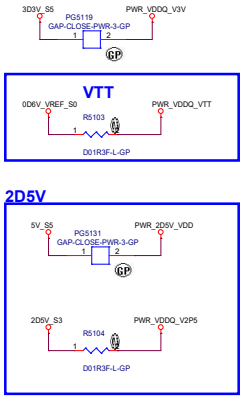
NB685GQ for VDDQ & VTT

https://minafix.com





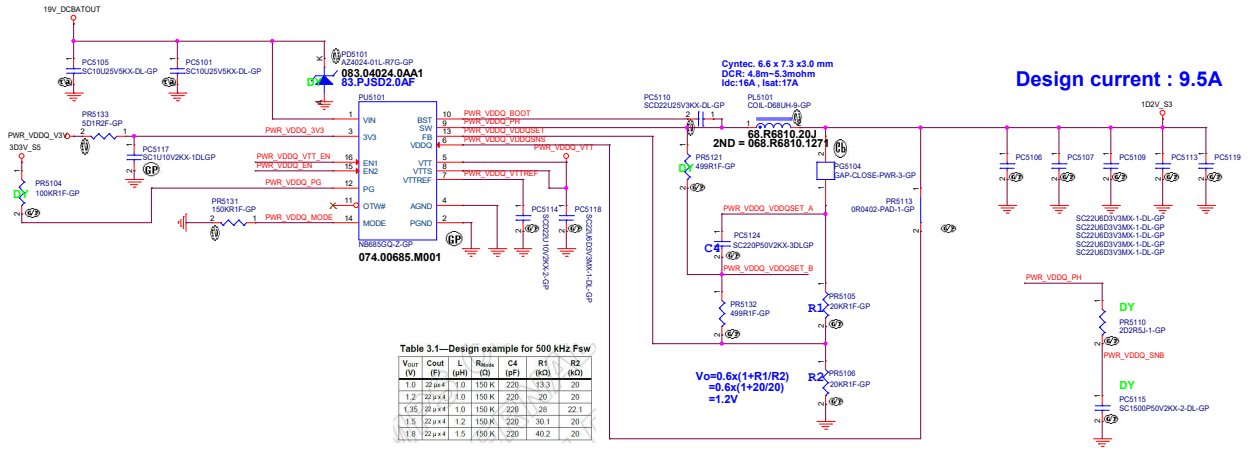
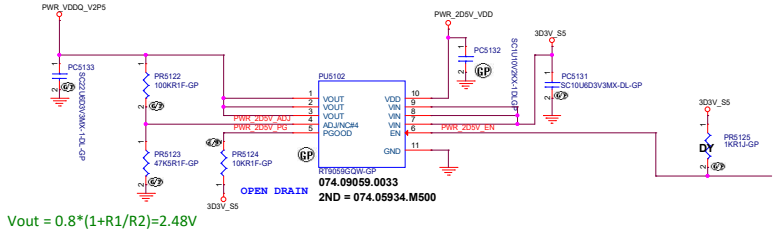


Table 3.1—Design example for 500 kHz Fsw

V_{OUT} (V)	Cout (F)	L (µH)	R_{fstdy} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)
1.0	22 µ x 4	1.0	150 K	220	13.3	20
1.2	22 µ x 4	1.0	150 K	220	20	20
1.35	22 µ x 4	1.0	150 K	220	28	22.1
1.5	22 µ x 4	1.2	150 K	220	30.1	20
1.8	22 µ x 4	1.5	150 K	220	40.2	20

Design Current = 0.84A

RT9059GQW for 2D5V



Vout = 0.8*(1+R1/R2)=2.48V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 051_Power (AOZ2260/VDD)

Size: Custom | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 51 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS54302_8V)

Size: A3 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 52 of 105

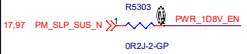
Main Func = 1D8V

OFFPAGE

OFFPAGE_GAP

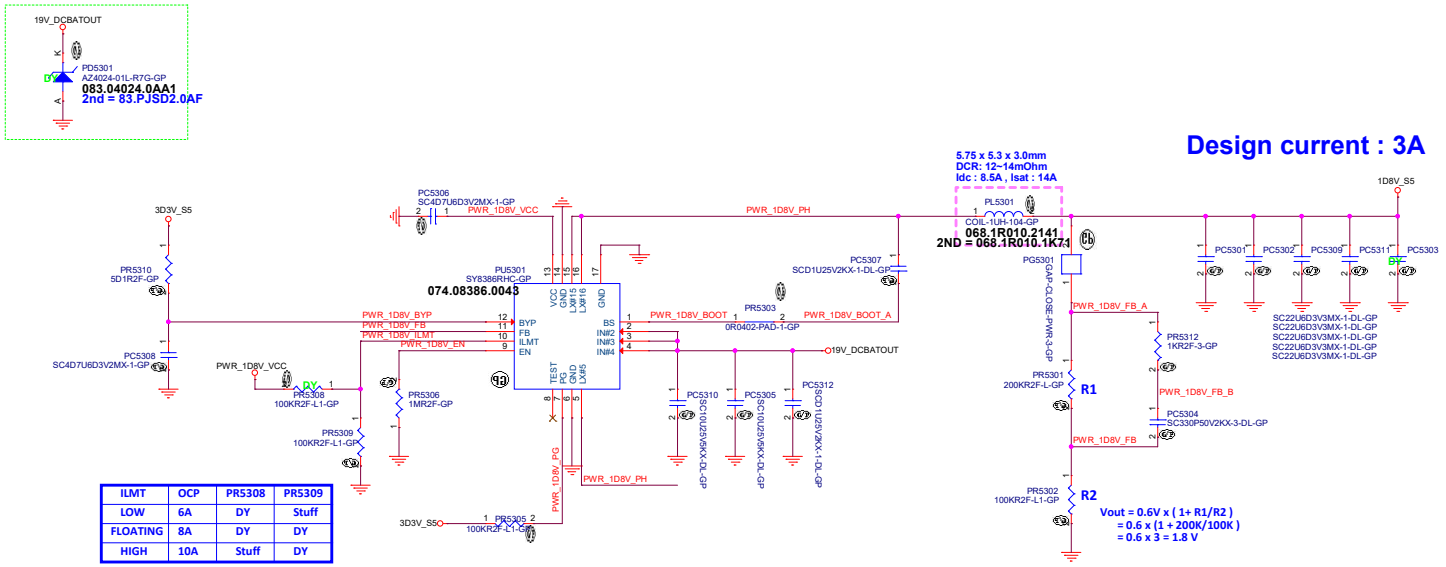
PH on EE Side

EE confirm



SY8386RHC for 1D8V

https://vinafix.com



ILMT	OCP	PR5308	PR5309
LOW	6A	DY	Stuff
FLOATING	8A	DY	DY
HIGH	10A	Stuff	DY

RT9081D for 1D8V_PROC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8883 1D8V		
Size: A2	Document Number: Odin ADL-P	Rev: SC
Date: Thursday, August 05, 2021	Sheet 53 of 105	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER(APW8738A_VNN1D05)

Size	Document Number	Rev
A3	Odin ADL-P	SC

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Main Func = LCD

- 4 eDP_TX_CPU_P2
- 4 eDP_TX_CPU_N2
- 4 eDP_TX_CPU_P1
- 4 eDP_TX_CPU_N1
- 4 eDP_TX_CPU_P2
- 4 eDP_TX_CPU_N2
- 4 eDP_TX_CPU_P3
- 4 eDP_TX_CPU_N3
- 4 eDP_AUX_CPU_P
- 4 eDP_AUX_CPU_N
- 4 eDP_HPD_CPU
- 4 eDP_VDD_EN
- 4 eDP_BLCTRL_CPU
- 24 LCD_TST
- 24 BLON_OUT
- 24 PANEL_MONITOR
- 24 LCD_VCC_TEST_EN
- 17,40,97 PM_SLP_S3_N
- 24 CABLE2_OCP#
- 16,55 CCD_USB20_P
- 16,55 CCD_USB20_N
- 20 GSEN_INT1_C
- 18 DBC_PANEL_EN
- 96 SENSOR_I2C_SDA_R
- 96 SENSOR_I2C_SCL_R
- 20,70,96 CPU_I2C_SDA_GSENSOR
- 20,70,96 CPU_I2C_SCL_GSENSOR

Main Func = Touch panel

- 20,96 CPU_I2C_SDA_TS
- 20,96 CPU_I2C_SCL_TS
- 18 TOUCH_PANEL_INT#_R
- 24 TOUCH_PANEL_EN_R
- 3 TOUCH_PANEL_DETECT#
- 4 TOUCH_PANEL_RST#_R

Main Func = CAMERA

- 16,55 CCD_USB20_N
- 16,55 CCD_USB20_P
- 27 DMIC_SCL_CODEC
- 27 DMIC_SDA_CODEC
- 19 DMIC_SCL_CPU
- 19 DMIC_SDA_CPU

RGB IR CAMERA

- 20 ALS_INT
- 20,96 CPU_I2C_SDA_IR
- 20,96 CPU_I2C_SCL_IR
- 3 IR_INT
- 18 IR_DET
- 4 CAMERA_2ND_DET

SIV Auto Test

- 96 CPU_I2C_SCL_TS_R
- 96 CPU_I2C_SDA_TS_R

Inverter Power

2nd = 69.02002.061
068.00002.2001
3RD = 69.02002.061

83.05315.0A0
2ND = 075.5V0X2.0070

69.50007.A31
2ND = 69.50007.G71

Brightness

75.00054.A7D
2ND = 75.00054.T7D

EC (BIST MODE)

ODIN N V

020.F0847.0040
2nd = 020.F1427.0040
3rd = 20.F2406.040

020.F0574.0050
2ND = 020.F0658.0050
3RD = 020.F1263.0050

eDP
Touch
Display
Camera & DMIC
Sensor Board

Hinge up cable protection

75.00054.A7D
2ND = 75.00054.T7D

074.02895.0A73
2ND = 074.05206.0093

3D3V_HINGE_R: FOR TOUCH MODULE

RGB IR Camera For Antman16

69.48001.081
2ND = 69.50011.081
3RD = 69.50013.061

Inverter Power

69.50007.A31
2ND = 69.50007.G71

ANT16

20.F1312.010

M-BIST/ LCD BIST

84.T3906.E11
2nd = 084.03906.0C11
3RD = 84.03906.R11

84.T3904.H11

VF=0.6V(IF=20mA)

83.R2003.A8M

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Scalar)

Size: C | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, September 09, 2010 | Sheet 35 of 58

Main Func = CRT

https://vinafix.com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT(Reserved)

Size: A3 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 56 of 105

SSID = HDMI Level Shifter/Connector

https://vinafix.com

4 HDMI_DDI_TX_N0
4 HDMI_DDI_TX_P0
4 HDMI_DDI_TX_N1
4 HDMI_DDI_TX_P1
4 HDMI_DDI_TX_N2
4 HDMI_DDI_TX_P2
4 HDMI_DDI_TX_N3
4 HDMI_DDI_TX_P3

4 HDMI_SCL_CPU
4 HDMI_SDA_CPU
4 HDMI_DET_CPU

SIV Auto Test

96 HDMI_SCL_CON
96 HDMI_SDA_CON

HDMI_DDI_TX_N3 C5701 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_P3 C5704 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_N0 C5705 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_P0 C5703 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_N1 C5707 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_P1 C5706 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_N2 C5708 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_P2 C5709 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P2

R5705 470R2F-GP
R5759 470R2F-GP
R5773 470R2F-GP
R5774 470R2F-GP
R5775 470R2F-GP
R5776 470R2F-GP
R5777 470R2F-GP
R5778 470R2F-GP

5V_S0
Q5701 2N7002KZ-2-GP-U
HDMI_PLL_GND
84.2N702.I31
4th = 084.07002.0C31
3rd = 084.27002.0L31
2ND = 084.27002.0N31

5V_S0
D5701 RB520S30-GP 83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F
D5702 RB520S30-GP 83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

3D3V_S0
RN5701 SRN4K7J-8-GP
HDMI_SCL_R
HDMI_SDA_R
3D3V_S0
RN5702 SRN2K2J-1-GP
HDMI_SCL_CPU
Part Reference = Q5702
HDMI_SCL_CON
HDMI_SDA_CPU
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C
HDMI_SDA_CON

HDMI_DDI_TX_CON_N0
20200410(DVT2)
Change to 180R
ER5701 180R2J-1-GP
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1
ER5702 180R2J-1-GP
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2
ER5703 180R2J-1-GP
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N3
ER5704 180R2J-1-GP
HDMI_DDI_TX_CON_P3

5V_S0
F5701 POLYSW-1D1A6V-9-GP-U 5V_HDMI
69.48001.081
2ND = 69.50011.081
3rd = 69.50013.061

20191122
Follow Nakia
20191127
For High limit
change back to follow ICL

HDMI CONN

5V_HDMI
20191218
For EMC required
SCD1U16V2KX-3DLGP EC5701
SCD1U16V2KX-3DLGP C5702

HDMI1
+5V_POWER
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
HDMI_SCL_CON
HDMI_SDA_CON
CEC
DDC/CEC_GROUND
HOT_PLUG_DETECT
RESERVED#14
GND
HDMI (A_Type)
SKT-HDMI23-278-GP
022.10025.0951
2nd = 022.10025.0961

3D3V_S0
Q5703 LMBT3904LT1G-GP
HDMI_HPD_B R5710 1 2 150KR2F-L-GP HDMI_DET_CON
HDMI_DET_CPU R5712 1 0R2J-2-GP HDMI_HPD_E
84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11
R5709 100KR2J-1-GP
R5711 200KR2F-L-GP

EMI Request:

ED5701 AZ1043-04F-R7G-GP
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
075.01043.0073
2ND = 075.08810.0A73
3rd = 075.73044.0003

ED5702 AZ1043-04F-R7G-GP
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
075.01043.0073

HDMI_DET_CON
ED5712 PESD5V0H1BSFYL-GP
083.5V0H1.00AF
2nd = 075.08315.0073
3rd = 083.05B75.00AM

HDMI_SCL_CON
ED5713 PESD5V0H1BSFYL-GP-U
083.5V0H1.00AF
2nd = 075.08315.0073
3rd = 083.05B75.00AM

HDMI_SDA_CON
ED5714 PESD5V0H1BSFYL-GP-U1
083.5V0H1.00AF
2nd = 075.08315.0073
3rd = 083.05B75.00AM

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (HDMI Conn/Retimer)
Size: A2
Document Number: Odin ADL-P
Rev: SC
Date: Thursday, August 05, 2021
Sheet 57 of 105

https://vinafix.com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*Odin ADL-P*	*SC*

Date: Thursday, August 05, 2021 Sheet 58 of 105

https://vinafix.com

(Blanking)

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***(Reserved)***		
Size: A4	Document Number: ***Odin ADL-P***	Rev: ***SC***
Date: Thursday, August 05, 2021	Sheet 59 of 105	

Main Func = HDD

HDD

HDD POWER

For Odin 15 L

https://vinafix.com

SATA RE-DRIVER

SATA HDD Connector

<Core Design>

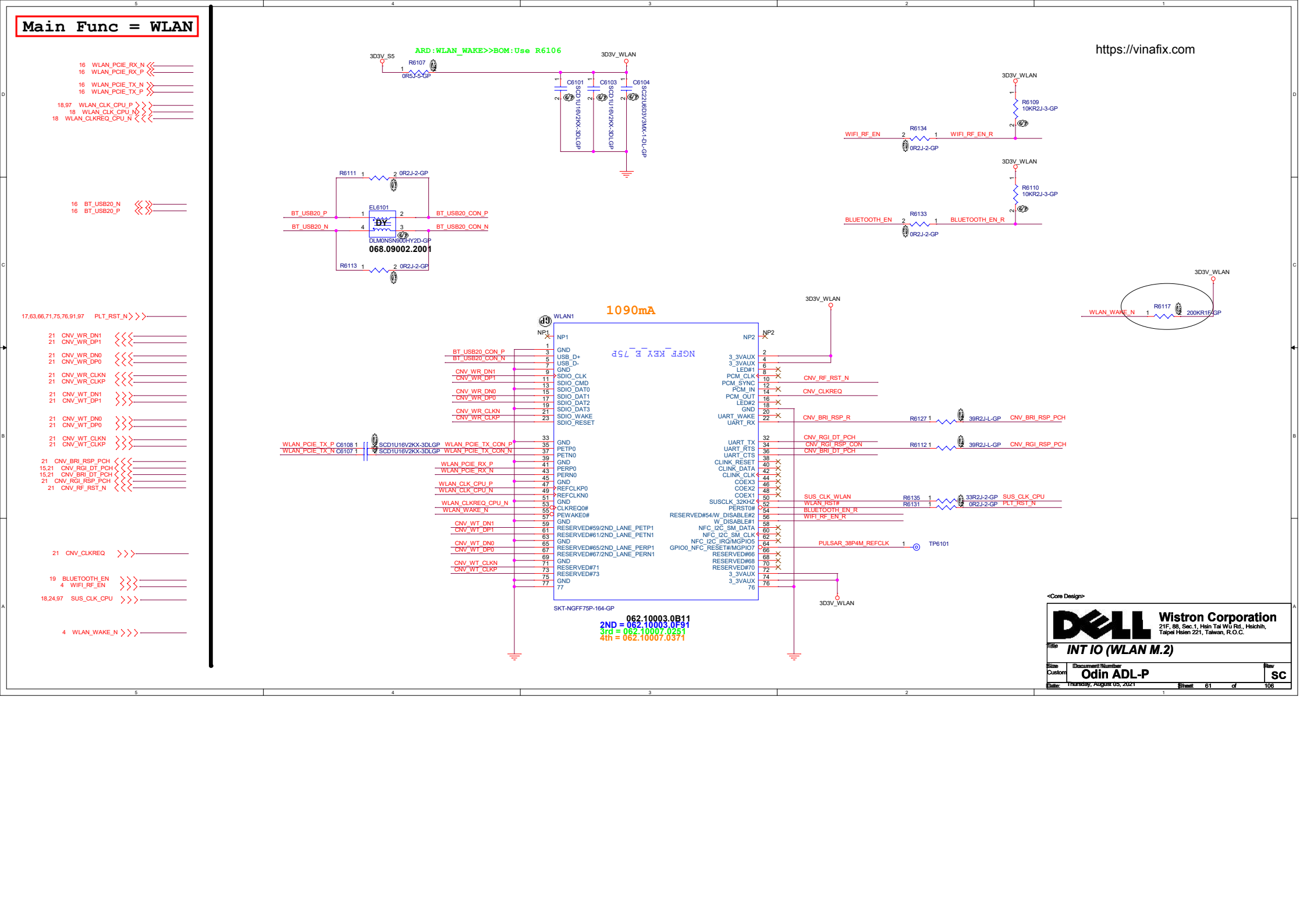
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF HDD/ODD

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 60 of 105

Main Func = WLAN



Main Func = WWAN

For Odin L

https://vinafix.com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

Size	Document Number	Rev
A4	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 62 of 105

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA

https://vinafix.com

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

Current Sense R

R6355 D01R5F-GP

C6305 SCD2P50V2JN-3DLGP
C6304 SCD2P50V2JN-3DLGP
C6306 SCD47U25V2KX-4GP
C6308 SCD47U25V2KX-4GP
C6307 SCD1U16V2KX-3DLGP
C6317 SC100U6D3VMX-DL-GP
C6318 SC100U6D3VMX-DL-GP
C6301 SC330U6V2KX-1DLGP

R6302 100KR2J-1-GP

SSD1_ALERT#

Reserve M.2 thermal report in CY21

PLT_RST_N — R6315 0R2J-2-GP — PLT_RST__SSD1_N

M2_PCIE_LED# — R6307 0R2J-2-GP — M2_PCIE_LED#_R

SSD_SCP# — R6306 0R2J-2-GP — SSD_SCP#_R

R6309 100KR2J-1-GP

SSD1_CLKREQ_CPU_N
PLT_RST__SSD1_N
SSD1_ALERT#
EC_I2C_SDA_SSD
EC_I2C_SCL_SSD
MSATA_DEVSLP1
AFTP6307 AFTE14P-1-GP

SSD M.2 CONN_Main

SSD1

NP2		NP1
NP2	76	77
76	74	75
3_3VAUX	72	GND 73
3_3VAUX	70	GND 71
3_3VAUX	68	GND 69 — M2_SSD_PEDET
SUSCLK_32KHZ	66	PEDET(OC_PCIE/GND_SATA) 67
NC#58	64	NC#67 57
NC#56	62	GND 55 — SSD1_CLK_CPU_P
PEWAKE#/NC#54	60	REFCLKP 53 — SSD1_CLK_CPU_N
CLKREQ#/NC#52	58	REFCLKN 51
PERST#/NC#50	56	GND 49 — SSD_PCIE_TX_C_P0 C6302 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_P0
NC#48	54	PERP0/SATA_A+ 47 — SSD_PCIE_TX_C_N0 C6303 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_N0
NC#46	52	PERN0/SATA_A- 45
NC#44	50	GND 43 — SSD1_PCIE_RX_P0
NC#42	48	PETP0/SATA_B- 41 — SSD1_PCIE_RX_N0
NC#40	46	PETN0/SATA_B+ 39
DEVSLP	44	GND 37 — SSD_PCIE_TX_C_P1 C6315 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_P1
NC#36	42	PERP1 35 — SSD_PCIE_TX_C_N1 C6316 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_N1
NC#34	40	PERN1 33
NC#32	38	GND 31 — SSD1_PCIE_RX_P1
NC#30	36	PETP1 29 — SSD1_PCIE_RX_N1
NC#28	34	PETN1 27
NC#26	32	GND 25 — SSD_PCIE_TX_C_P2 C6313 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_P2
NC#24	30	PERP2 23 — SSD_PCIE_TX_C_N2 C6314 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_N2
NC#22	28	PERN2 21
NC#20	26	GND 19 — SSD1_PCIE_RX_P2
3_3VAUX	24	PETN2 17 — SSD1_PCIE_RX_N2
3_3VAUX	22	PETP2 15
3_3VAUX	20	GND 13 — SSD_PCIE_TX_C_P3 C6311 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_P3
3_3VAUX	18	PERP3 11 — SSD_PCIE_TX_C_N3 C6312 1 — SCD22U10V2KX-2-GP — SSD1_PCIE_TX_N3
DAS/DSS#	16	PERN3 9
NC#8	14	GND 7 — SSD1_PCIE_RX_P3
NC#6	12	PETN3 5 — SSD1_PCIE_RX_N3
3_3VAUX	10	PETP3 3
3_3VAUX	8	GND 1
	6	GND GP
	4	
	2	

NGFF_KEY_M 75P

SKT-NGFF75P-146-GP-U

062.10003.00A1
2ND = 062.10003.0411
3RD = 062.10003.0991

R6305 10KR2J-3-GP

AFTP6304 AFTE14P-1-GP

24 EC_I2C_SDA_SSD
24 EC_I2C_SCL_SSD
17,61,66,71,75,76,91,97 PLT_RST_N
3 M2_PCIE_LED#
24 SSD_SCP#
24 SSD1_ALERT#

SSD1

18 SSD1_CLK_CPU_P
18 SSD1_CLK_CPU_N
18 SSD1_CLKREQ_CPU_N
16 SSD1_PCIE_TX_P3
16 SSD1_PCIE_TX_N3
16 SSD1_PCIE_RX_P3
16 SSD1_PCIE_RX_N3
16 SSD1_PCIE_TX_P2
16 SSD1_PCIE_TX_N2
16 SSD1_PCIE_RX_P2
16 SSD1_PCIE_RX_N2
16 SSD1_PCIE_TX_P1
16 SSD1_PCIE_TX_N1
16 SSD1_PCIE_RX_P1
16 SSD1_PCIE_RX_N1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)

Size: Custom | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet: 63 of 105

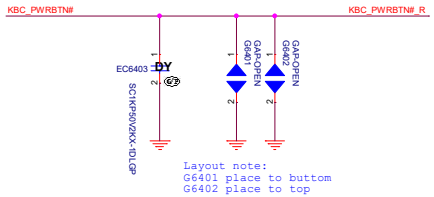
Main Func = Power BTN

24,66 KBC_PWRBTN#

24,66 KBC_PWRBTN#_R

Power button

https://vinafix.com



Main Func = Battery LED

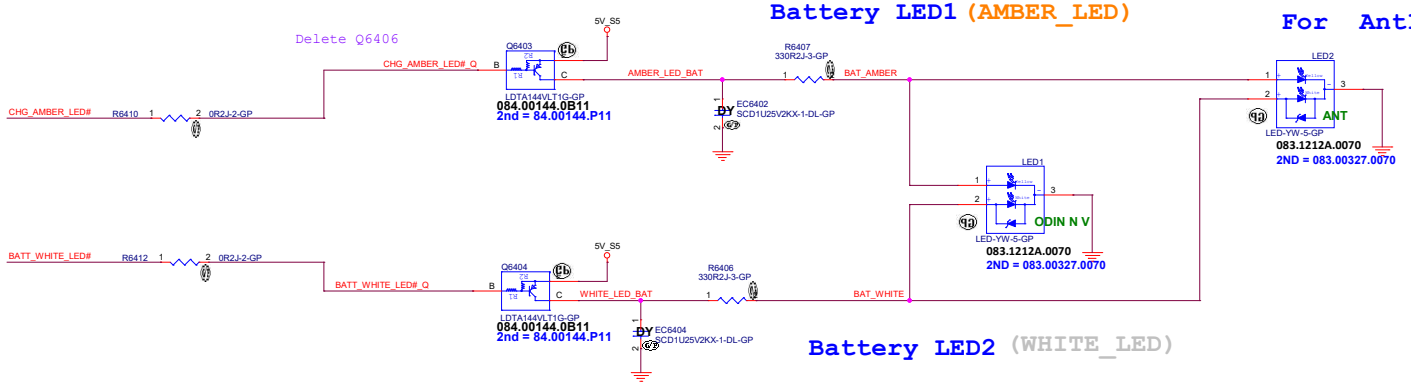
Low actived from KBC GPIO

24 CHG_AMBER_LED#

3,24 BATT_WHITE_LED#

Battery LED1 (AMBER_LED)

For Ant14/16

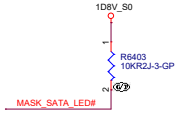


Battery LED2 (WHITE_LED)

Main Func = HDD LED

3,24 MASK_SATA_LED#

SATA HDD LED
LOW actived from PCH GPIO

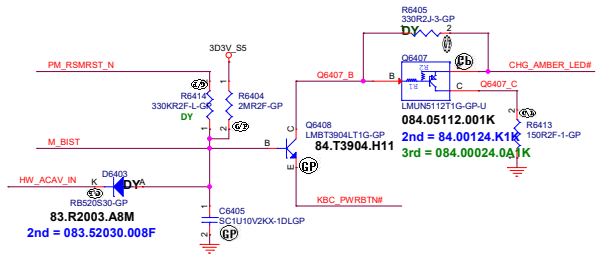


Main Func = M-BIST

17,97 PM_RSMRST_N

24 M_BIST

24,44 HW_ACAV_IN



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 64 of 105

Main Func = KB

24 CAP_LED#_R

4 KB_DET#

20 KB_LED_BL_DET

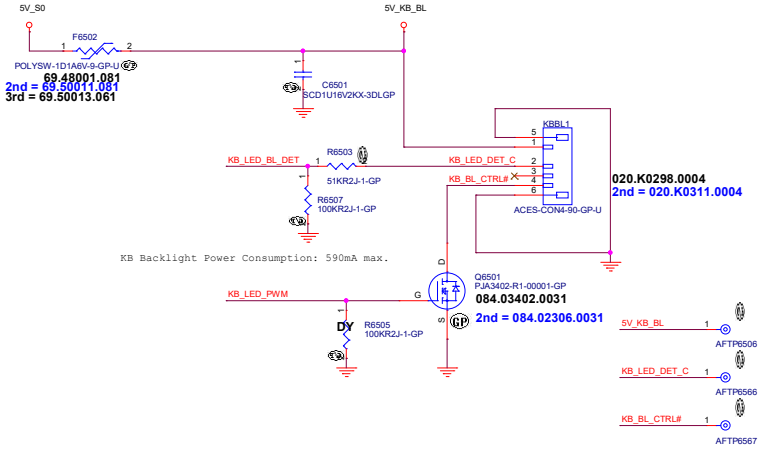
24 KB_LED_PWM

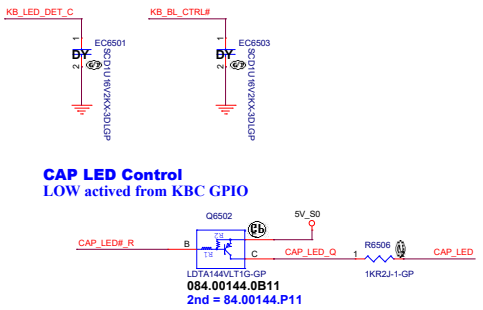
24 KSO00
24 KSO01
24 KSO02
24 KSO03
24 KSO04
24 KSO05
24 KSO06
24 KSO07
24 KSO08
24 KSO09
24 KSO10
24 KSO11
24 KSO12
24 KSO13
24 KSO14
24 KSO15
24 KSO16

24 KSI[0..7]

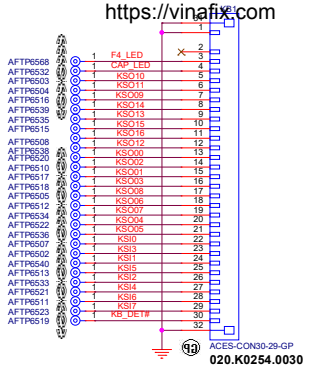
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7

Keyboard Backlight





Internal Keyboard Connector



https://vinafix.com

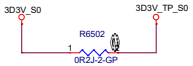
Main Func = TPAD

24 EC_I2C_SDA_TP
24 EC_I2C_SCL_TP

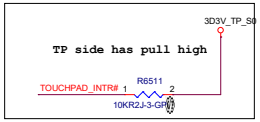
20,66 CPU_I2C_SCL_TP
20,66 CPU_I2C_SDA_TP

18,24 TOUCHPAD_INTR#
24 PTP_DIS#

SIV Auto Test



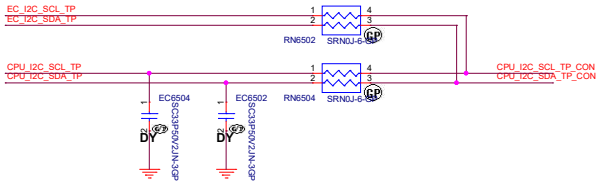
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

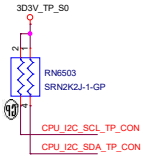


Support PTP

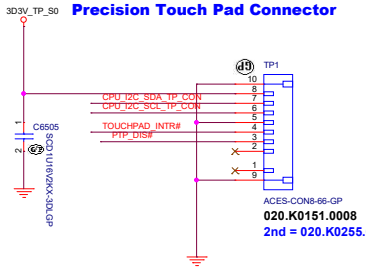
PS2

I2C





Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 65 of 105

IO Board Connector (Colay)

https://vinafix.com

Main Func = IO Connector

IO DET

AUDIO
- 27,29 AUD_RING
- 27,29 AUD_SLEEVE
- 29 AUD_HP1_JACK_L1
- 29 AUD_HP1_JACK_R1
- 27 AUD_HPJD_N

CRD
- 16 CARD1_USB20_N
- 16 CARD1_USB20_P

USB3.0

PORT2
- 16 USB4_USB30_RX_N
- 16 USB4_USB30_RX_P
- 16 USB4_USB30_TX_N
- 16 USB4_USB30_TX_P
- 16 USB4_USB20_N
- 16 USB4_USB20_P

PORT3 FOR L

USB CONTROL
- 16 USB_OC3_N
- 24,35 USB_PWR_EN#

LAN
- 16 LAN_PCIE_RX_N
- 16 LAN_PCIE_RX_P
- 16 LAN_PCIE_TX_N
- 16 LAN_PCIE_TX_P
- 16 LAN_CLK_CPU_N
- 16 LAN_CLK_CPU_P
- 18 LAN_CLKREQ_CPU_N
- 24 LAN_ENABLE
- 24 PCH_LAN_WAKE_N

FP
- 16 FP1_USB20_N
- 16 FP1_USB20_P
- 24 FPR_SCAN#
- 24,64 KBC_PWRBTN#_R
- 17,51,97 PM_SLP_S4_N

- 20,24 LID_CL_SIO#
- 24 LID_POWER_ON#
- 3,24 LID_CL_SIO_TAB#
- 3,6,7,8,71,75,76,91,97 PLT_RST_N
- 20,65 CPU_I2C_SCL_TP
- 20,65 CPU_I2C_SDA_TP
- 7,61,63,66,71,75,76,91,97 PLT_RST_N
- 18 CR_IC_DET#
- 24,44 PBAT_PRES#
- 16,19 SIZE_ID1

IO USB POWER 2A

Pin define by follow layout routing

Layout Note:
Need to Close CON

5V_S5 → C6601 22U/6.3V/X5R/0603 → U6021 G524B2T11U-GP (IN, EN#, OUT, GND, OC#) → USB_OC3_N

USB_PWR_EN# → R6622 10K/F

OUSB30_VCCC → C6606 22U/6.3V/X5R/0603, C6607 22U/6.3V/X5R/0603, C6608 22U/6.3V/X5R/0603, C6609 0.1U/16V/X7R/0402

074.00524.0C9F
2nd = 074.03003.007G
3rd = 074.07115.0B9F

LID sensor

LID_CL_SIO# → D6601 RB520S30-GP → LID_CL_N8# → R6627 680K/F → Q6701_G

C6804 SCD1U16V2KX-3DLGP

LID_POWER_ON# → C6805 SC47UD3V2MX-1-GP

Q6601 2N7002KW-1-GP

R6628 680K/F → 3D3V_AUX_S5

C6803 SC1U10V2KX-1DLGP

D6602 RB520S30-GP → Q6701_G_D

83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

75.27002.F7C
2nd = 075.27002.007C
3rd = 075.67002.007C

CARD

CARD1_USB20_N / CARD1_USB20_P → R6604 0R2J-2-GP → CARD1_USB20_CON_N / CARD1_USB20_CON_P

DLM0NSN900HY2DGP EL6601

068.09002.2001
2nd = 68.02002.061

R6605 0R2J-2-GP

USB3.0 PORT1

USB4_USB20_N / USB4_USB20_P → R6608 0R2J-2-GP → USB4_USB20_CON_N / USB4_USB20_CON_P

DLM0NSN900HY2DGP EL6603

068.09002.2001
2nd = 68.02002.061

R6610 0R2J-2-GP

FP

FP1_USB20_N / FP1_USB20_P → R6506 0R2J-2-GP → FP1_USB20_CON_N / FP1_USB20_CON_P

DLM0NSN900HY2DGP EL6502

068.09002.2001
2nd = 68.02002.061

R6507 0R2J-2-GP

FINGER PRINTER

Card Reader

USB3.1 PORT1

RTC

3D3V_S0 → R6617 100K/F1-GP → CR_IC_DET#

BATT_RTC → R6615 100K/F2.1-1-GP → LID_CL_SIO_TAB#_R → Q6603 PJT138KA-GP → LID_CL_SIO_TAB# → R6616 100K/F2.1-1-GP → 1D8V_S5

R6613 2M/F2P-GP

075.00138.0A7C
2nd = 075.00139.007C
3rd = 075.00138.0B7C

PBAT_PRES# → R6612 0R2J-2-GP → PBAT_PRES#_R

AUDIO

AUD_HP1_JACK_L1 / AUD_HP1_JACK_R1 / AUD_HPJD_N / AUD_SLEEVE / AUD_RING → AUD_AGND

FINGER PRINTER

FP1_USB20_CON_N / FP1_USB20_CON_P / LID_CL_SIO# / FPR_SCAN#

Card Reader

CR_IC_DET# / CARD1_USB20_CON_N / CARD1_USB20_CON_P

USB3.1 PORT1

USB4_USB20_CON_N / USB4_USB20_CON_P / USB4_USB30_TX_P / USB4_USB30_TX_N / USB4_USB30_RX_P / USB4_USB30_RX_N

PM_SLP_S4_N / KBC_PWRBTN#_N

RTC

3D3V_RTC_VCC / 3D3V_S0 / 3D3V_S5 / 3D3V_AUX_S5

LANWAKE# / USB30_VCCC / PLT_RST_N

IO3D3 → ODIN N ANT → STAR-CON40-8-GP

020.F0847.0040
2ND = 020.F1427.0040
3RD = 020.F2406.040

AUDIO

AUD_HP1_JACK_L1 / AUD_HP1_JACK_R1 / AUD_HPJD_N / AUD_SLEEVE / AUD_RING → AUD_AGND

FINGER PRINTER

FP1_USB20_CON_N / FP1_USB20_CON_P / LID_CL_SIO# / FPR_SCAN#

Card Reader

CR_IC_DET# / CARD1_USB20_CON_N / CARD1_USB20_CON_P

USB3.1 PORT1

USB4_USB20_CON_N / USB4_USB20_CON_P / USB4_USB30_TX_P / USB4_USB30_TX_N / USB4_USB30_RX_P / USB4_USB30_RX_N

PM_SLP_S4_N / KBC_PWRBTN#_N

RTC

3D3V_RTC_VCC / 3D3V_S0 / 3D3V_S5 / 3D3V_AUX_S5

LID_CL_SIO_TAB#_R → R6609 0R2J-2-GP → 2IN1

PCH_LAN_WAKE_N → R6611 0R2J-2-GP → ODIN V

SIZE_ID1 → R6614 0R1J-GP → ODIN N

LANWAKE# / USB30_VCCC / PLT_RST_N

LAN

LAN_PCIE_RX_N / LAN_PCIE_RX_P / LAN_PCIE_TX_N / LAN_PCIE_TX_P / LAN_CLK_CPU_P / LAN_CLKREQ_CPU_N / LAN_ENABLE

IO3D1 → IPEX-CON50-1-GP → ODIN V

020.F0574.0050
2ND = 020.F0688.0050

TP6601 TP6602 → 19V_DCBATOUT_E3 / 19V_DCBATOUT_LCD_R_E3

TP6603 TP6604 → 3D3V_LCDVDD_R_E3 / 3D3V_LCDVDD_S0_E3

TP6605 TP6606 → 3D3V_SSD1_E3_R / 3D3V_SSD1_E3

TP6607 TP6608 → 19V_CHARGER_E3

TP6609 TP6610 → 19V_VCOREA_E3 / PWR_VCOREA_E3

TP6611 TP6612 → 19V_VCCIN_AUX_E3 / PWR_VCCIN_AUX_E3

TP6613 TP6614 → 3D3V_SS_E3 / 3D3V_WLAN_E3

TP6615 TP6616 → 19V_VDDQ_E3 / PWR_VDDQ_E3

CN → 20.F1450.020

WLAN input	IN1+	3D3V_SS_E3	IN4+ LCD BACKLIGHT
	IN1-	3D3V_WLAN_E3	IN4-
IN2+	3D3V_SSD1_E3_R		IN3+ Panel logic power
SSD IN2-		3D3V_SSD1_E3	IN3-
	IN7-	PWR_VDDQ_E3	IN6-
VDDQ input	IN7+	19V_VDDQ_E3	IN6+ CPU Core input
	IN8-	PWR_VCCIN_AUX_E3	IN5-
VCCIN AUX input	IN8+	19V_VCCIN_AUX_E3	IN5+ System power source

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Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3 | Document Number: Odin ADL-P | Rev: SC
Date: Thursday, August 05, 2021 | Sheet 68 of 105

Main Func = HALL SENSOR

https://vinafix.com

<Core Design>

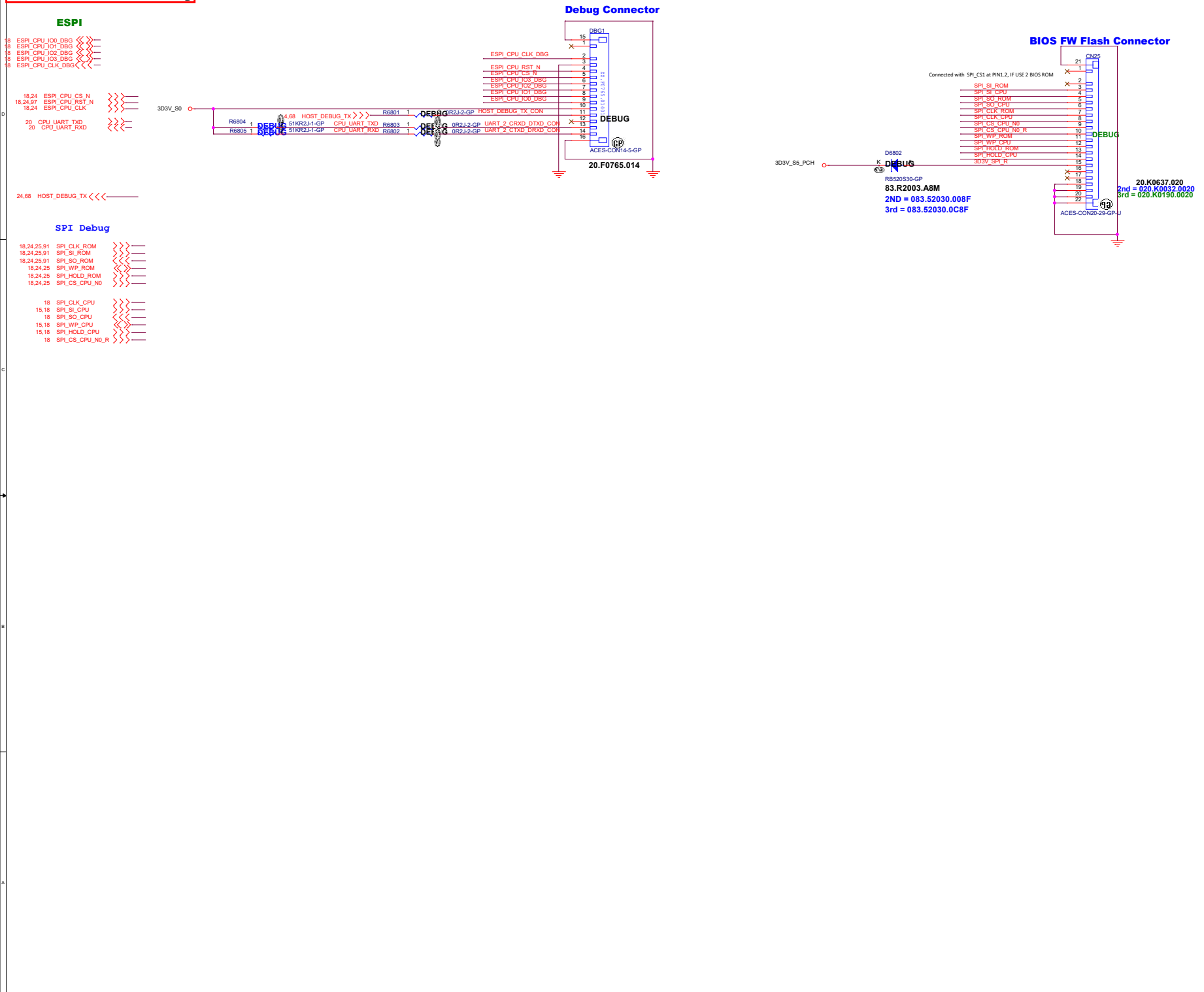
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Odin ADL-P* | Rev: *SC*

Date: Thursday, August 05, 2021 | Sheet 67 of 105

Main Func = Debug



https://vinafix.com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC debug)

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 68 of 105

https://vinafix.com

(Blanking)

<Core Design>

Wistron Corporation
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Title

Reserved

Size	Document Number	Rev
A4	Odin ADL-P	SC

Date: Thursday, August 05, 2021 Sheet 69 of 105

SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

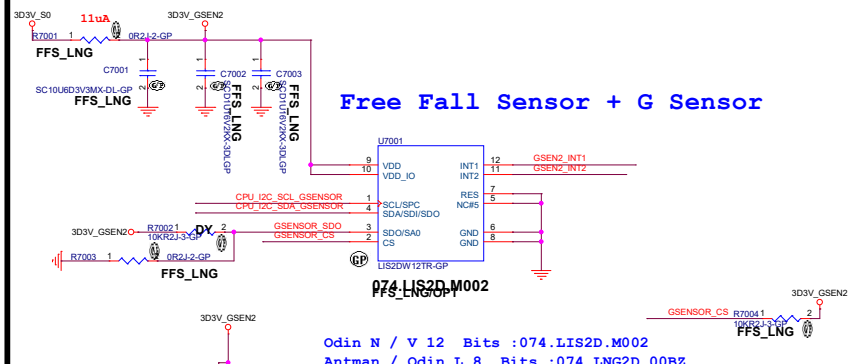
https://vinafix.com

20,55,96 CPU_I2C_SDA_GSENSOR
20,55,96 CPU_I2C_SCL_GSENSOR

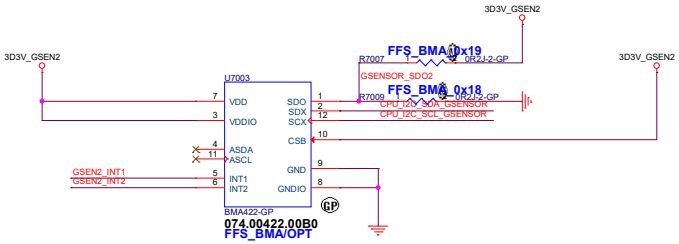
20 GSEN2_INT1_C
20 GSEN2_INT2_C

24 CPU_I2C_SDA_SAR
24 CPU_I2C_SCL_SAR

Free Fall Sensor + G Sensor



Odin N / V 12 Bits :074.LIS2D.M002
Antman / Odin L 8 Bits :074.LNG2D.00BZ



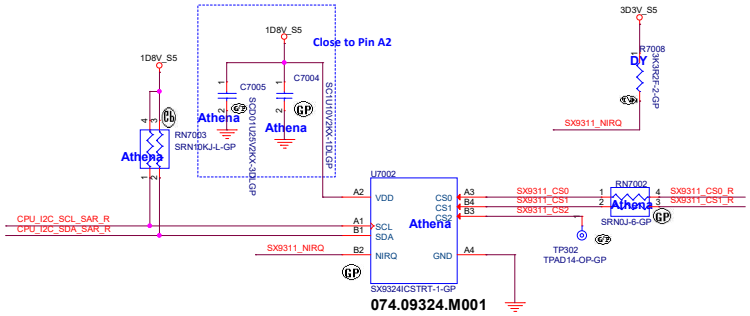
The default I2C address of the device is 0b00011000 (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0b00011001 (0x19) is selected by pulling the SDO pin to 'VDDIO'.

Odin N / V 12 Bits :074.00456.M003
Antman / Odin L 8 Bits :074.00422.00B0

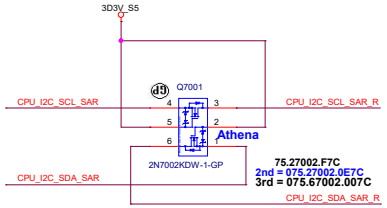
Note:

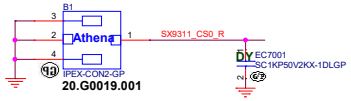
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

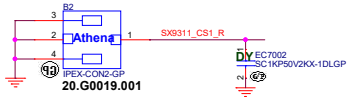
P-SENSOR for ANT16



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A2 | Document Number: Odin ADL-P | Rev: SC

Date: Thursday, August 05, 2021 | Sheet 70 of 105

Main Func = TBT

RF team on applying, only murata have sample can meet Intal request
220nF AC cap must be placed on RX lines close to SOC side

	WPN	DPN
TBT 8040	https://www.fixcom	M11GX
NON TBT 8010	071.00TBT.0D0U	7DYVG
PS8828-A2	071.08828.0C0U	

TBT PORTS

BB TO PCH(TBT)

SMBUS	SMBUS_SCL	For non-vPro® support on TBT™ ports, leave SMBus pins open. For Intel vPro® support on TBT™ ports, connect SMBus pins to PCH SML0. SMBus need to pull up to system 3.3V Sx power rail on PCH side.
	SMBUS_SDA	

R7112
8010/8040 : 4.75K 64.47516.6DL
PS8828 : 4.99K 64.49915.6DL

BB1/OPT

BB1/8010

072.25Q80.0C01
2nd = 072.25835.M001
3rd = 072.02580.0A0D
1MB Flash ROM

BB1/8010_2PORT/PS8828

L: Set Re-timer to be Slave on shared flash SPI I/F
H: Set Re-timer to be Master on shared flash SPI I/F

H: Flash is shared between 2 Re-timers

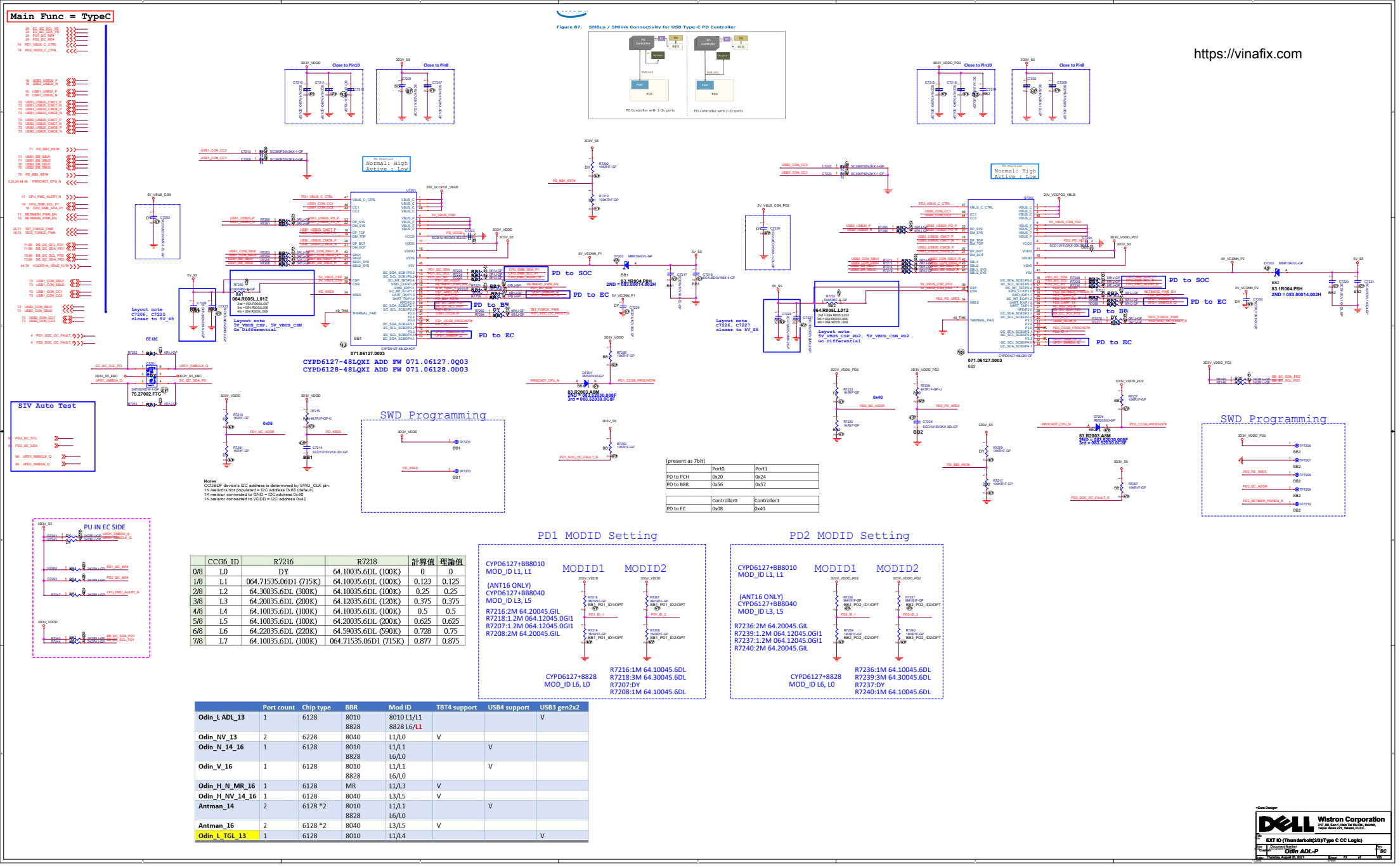
	BB_TCP1_FLASH_SHARE_EN	BB_TCP1_FLASH_MSTR_SLV
H	FLASH SHARE ENABLE	MASTER MODE
L	FLASH SHARE DISABLE	SLAVE MODE

INTEL Recommend
20200406 from Stradale

074.22975.0093
2ND = 74.03526.093

068.R6810.1201
2nd = 068.R6810.1471
3rd = 068.R6810.1141

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title:	EXT IO (Thunderbolt(1/3)/Type C Re-driver)
Size: A1	Document Number: Odin ADL-P
Rev: SC	
Date: Thursday, August 05, 2021	Sheet 71 of 103



(present as 7bit)	Port0	Port1
PD to PCH	0x20	0x24
PD to BBR	0x56	0x57

	Controller0	Controller1
PD to EC	0x08	0x40

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

PD1 MODID Setting

CYPD6127+BB8010
MOD_ID L1, L1

(ANT16 ONLY)
CYPD6127+BB8040
MOD_ID L3, L5

R7216:2M 64.20045.GIL
R7218:1.2M 064.12045.0GI1
R7207:1.2M 064.12045.0GI1
R7208:2M 64.20045.GIL

MODID1 / MODID2

CYPD6127+8828
MOD_ID L6, L0

R7216:1M 64.10045.6DL
R7218:3M 64.30045.6DL
R7207:DY
R7208:1M 64.10045.6DL

PD2 MODID Setting

CYPD6127+BB8010
MOD_ID L1, L1

(ANT16 ONLY)
CYPD6127+BB8040
MOD_ID L3, L5

R7236:2M 64.20045.GIL
R7239:1.2M 064.12045.0GI1
R7237:1.2M 064.12045.0GI1
R7240:2M 64.20045.GIL

MODID1 / MODID2

CYPD6127+8828
MOD_ID L6, L0

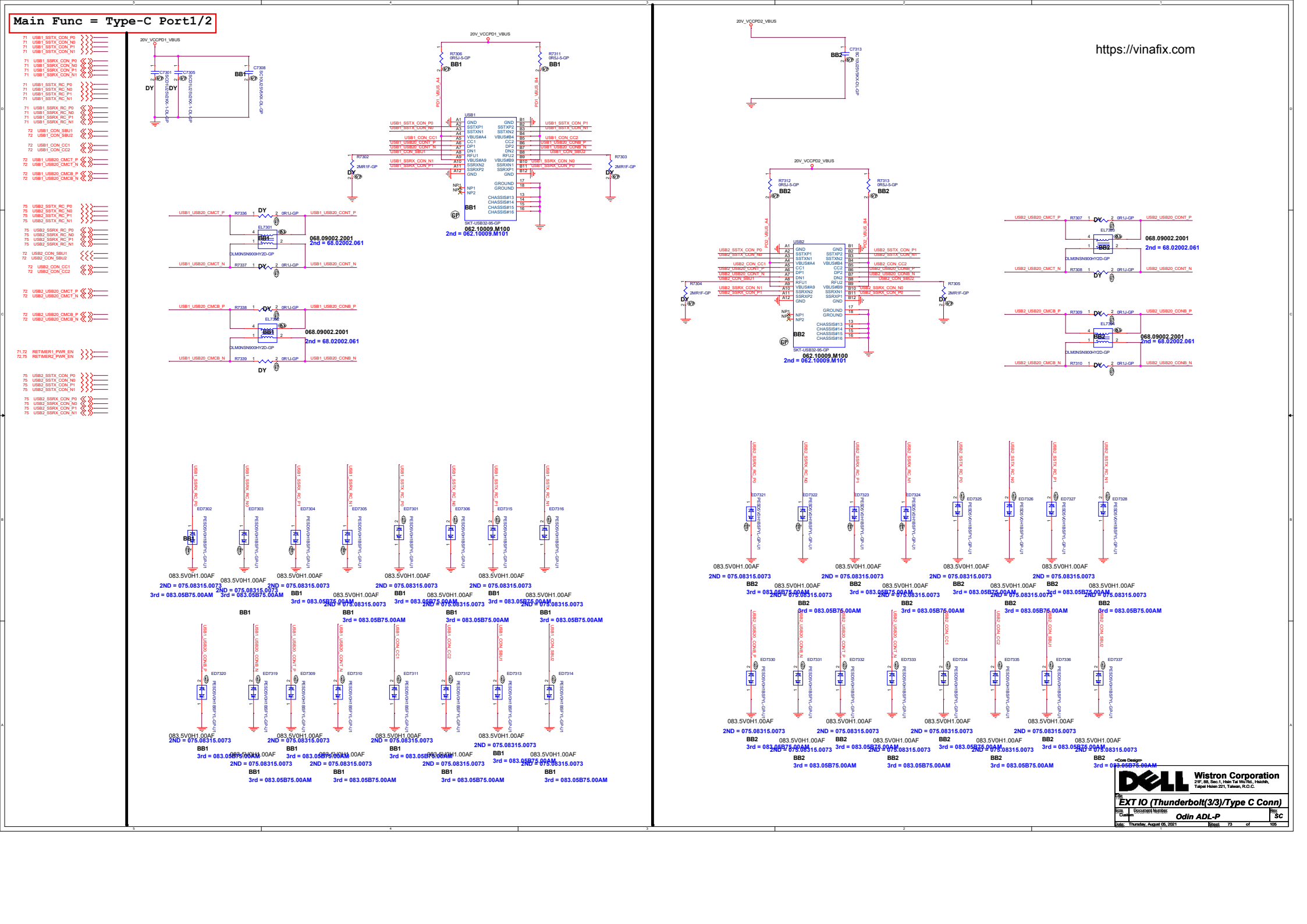
R7236:1M 64.10045.6DL
R7239:3M 64.30045.6DL
R7237:DY
R7240:1M 64.10045.6DL

	Port count	Chip type	BBR	Mod ID	TBT4 support	USB4 support	USB3 gen2x2
Odin_L ADL_13	1	6128	8010	8010 L1/L1			V
			8828	8828 L6/L1			
Odin_NV_13	2	6228	8040	L1/L0	V		
Odin_N_14_16	1	6128	8010	L1/L1		V	
			8828	L6/L0			
Odin_V_16	1	6128	8010	L1/L1		V	
			8828	L6/L0			
Odin_H_N_MR_16	1	6128	MR	L1/L3	V		
Odin_H_NV_14_16	1	6128	8040	L3/L5	V		
Antman_14	2	6128 *2	8010	L1/L1		V	
			8828	L6/L0			
Antman_16	2	6128 *2	8040	L3/L5	V		
Odin_L_TGL_13	1	6128	8010	L1/L4			V

Wistron Corporation
EXT IO (Thunderbolt(3)/Type C CC Logic)
Odin ADL-P

Main Func = Type-C Port1/2

https://vinafix.com

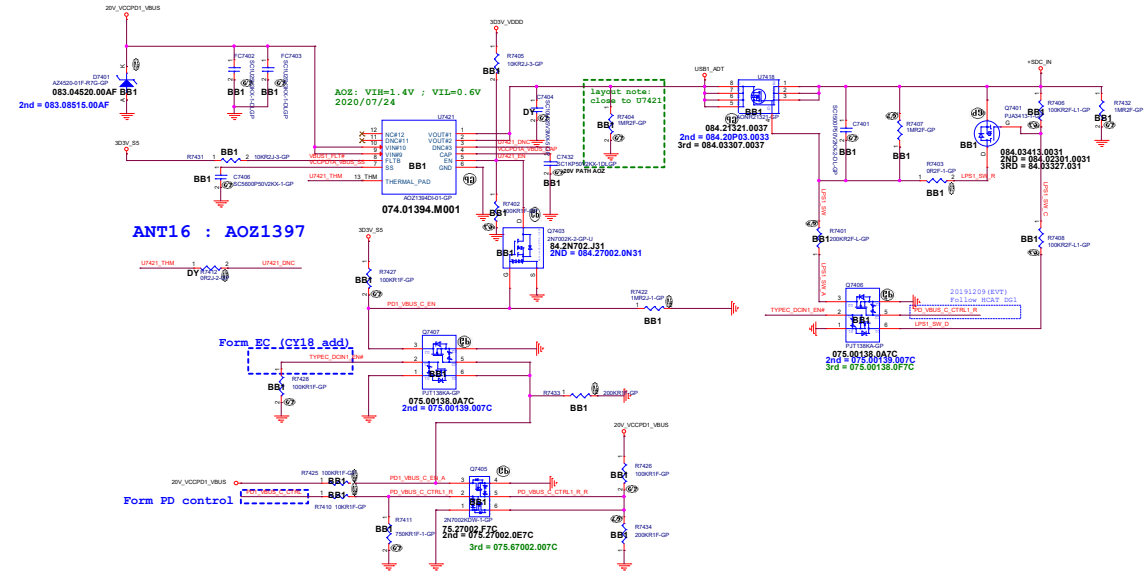


Main FUNC = LPS

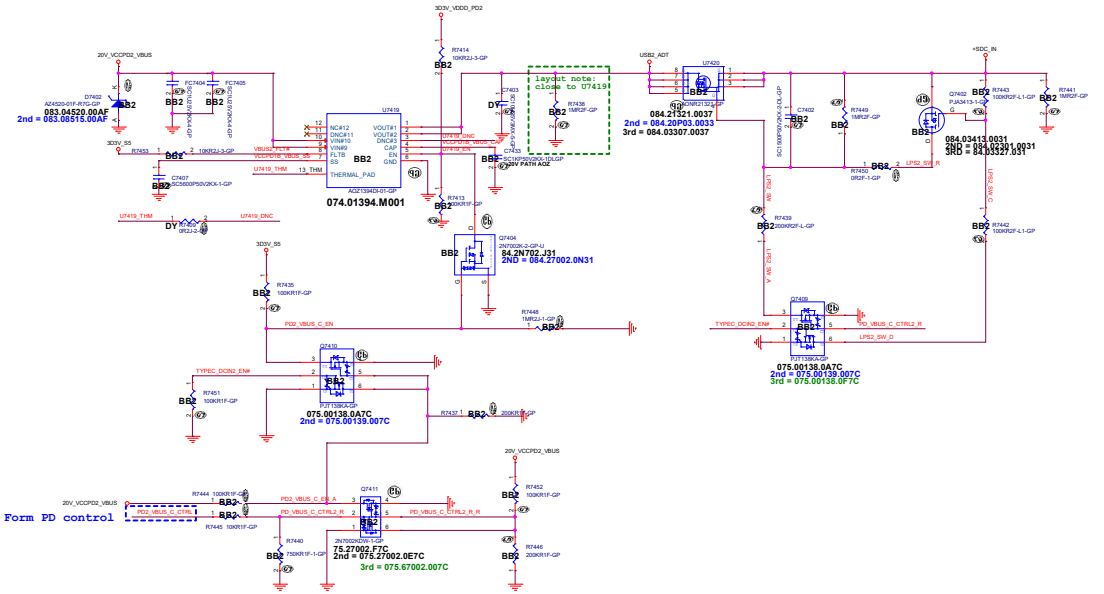
https://vinafix.com

72 PD1_VBUS_C_CTRL
72 PD2_VBUS_C_CTRL
24 TYPEC_DCIN1_ENF
24 TYPEC_DCIN2_ENF
44 VCCPD1A_VBUS_FLT#

TYPE-C Port 1



TYPE-C Port 2



<Core Design>

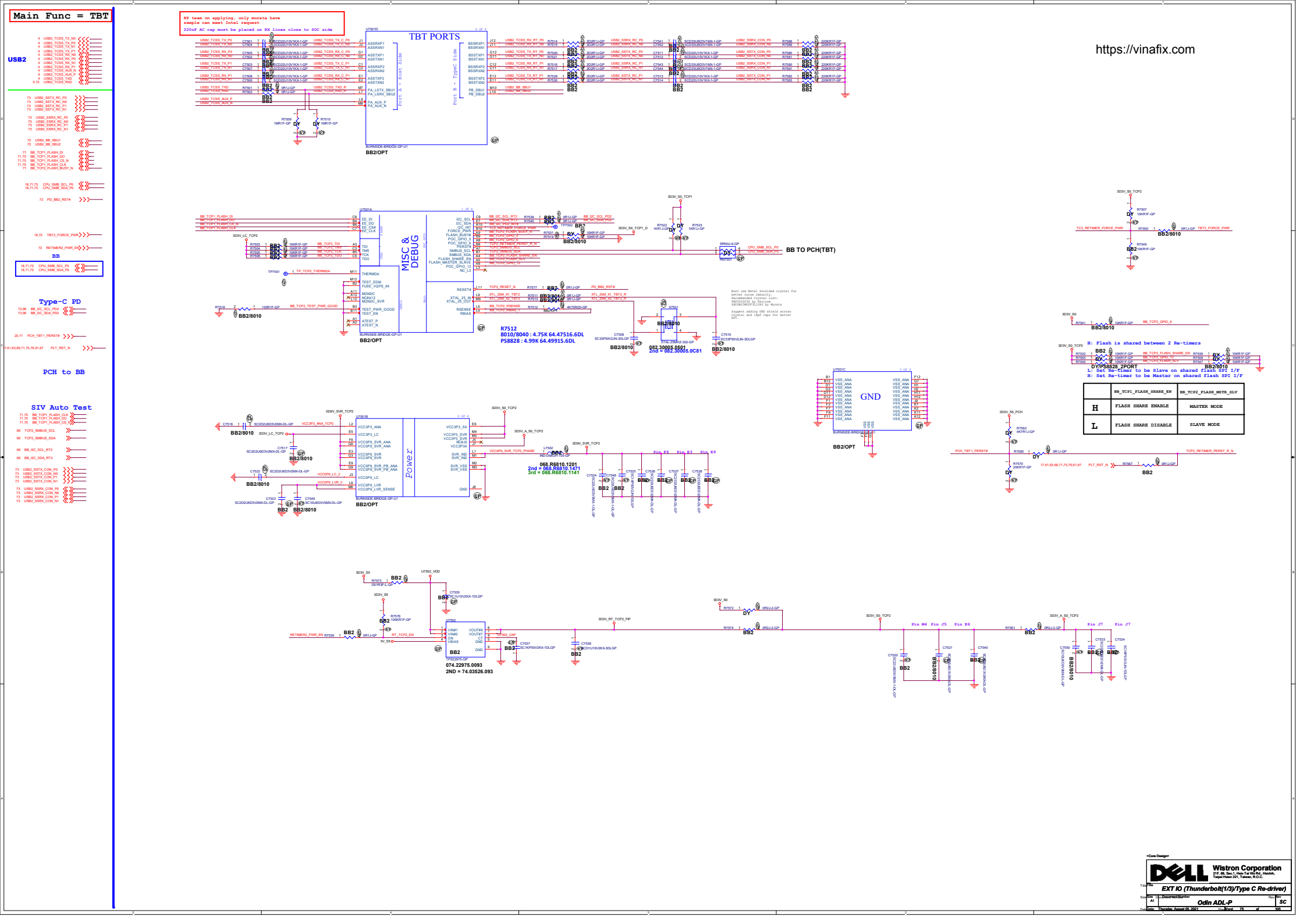
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO(LPS)

Size: A3 | Document Number | Rev

Date: Thursday, August 06, 2020 | Sheet 74 of 93

Odin ADL-P SC


Main Func = TBT
RF team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side
TBT PORTS
Port B - Type-C Side
Port A - Host Side
BURNSIDE-BRIDGE-GP-U1
BB2/OPT
MISC & DEBUG
BB TO PCH(TBT)
R7512
8010/8040 : 4.75K 64.47516.6DL
PS8828 : 4.99K 64.49915.6DL
Must use Metal shielded crystal for better noise immunity.
Recommended Crystal List:
082300250 by Perlcom
XRCGB25M000F1128S by Murata
Suggest adding GND shield across crystal and 18pF caps for better EMI.
Power
GND
H: Flash is shared between 2 Re-timers
L: Set Re-timer to be Slave on shared flash SPI I/F
H: Set Re-timer to be Master on shared flash SPI I/F
DYPS8828_2PORT
BB_TCP1_FLASH_SHARE_EN
BB_TCP2_FLASH_MSTR_SLV
H
FLASH SHARE ENABLE
MASTER MODE
L
FLASH SHARE DISABLE
SLAVE MODE
https://vinafix.com
Wistron Corporation
EXT IO (Thunderbolt(1/3)/Type C Re-driver)
Odin ADL-P
SC

GN18-S5 071.0GN18.0B0U
GN20-S5 071.0GN20.0N0U

https://vinafix.com

6,24,85 DGPU_PWROK

18 GFX_CLK_CPU_P
18 GFX_CLK_CPU_N
18 GFX_CLKREQ_CPU_N

6 DGPU_HOLD_RST_N

16 GFX_PCIE_RX_P0
16 GFX_PCIE_RX_N0
16 GFX_PCIE_TX_P0
16 GFX_PCIE_TX_N0

16 GFX_PCIE_RX_P1
16 GFX_PCIE_RX_N1
16 GFX_PCIE_TX_P1
16 GFX_PCIE_TX_N1

16 GFX_PCIE_RX_P2
16 GFX_PCIE_RX_N2
16 GFX_PCIE_TX_P2
16 GFX_PCIE_TX_N2

16 GFX_PCIE_RX_P3
16 GFX_PCIE_RX_N3
16 GFX_PCIE_TX_P3
16 GFX_PCIE_TX_N3

85,86 1V_VGA_S0_PG

85,86 PWR_VGA_NVVDDS_PG

17,61,63,66,71,75,91,97 PLT_RST_N

79 SYS_PEX_RST_MON_N

EMI Reserved

GPU_PEX_RST_N

EC7601 SC3P50V2JN-3DGBP

DY

▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.

dGPU Reset

1D8V_AON_S0

DGPU_HOLD_RST_N

PLT_RST_N

U7601 TC7SZ08FU-LJ-CT-GP

R7607 10KR1J-GP

SYS_PEX_RST_MON_N

R7606 100KR1J-GP

073.7SZ08.000G
2nd = 73.7SZ08.DAH
3rd = 73.01G08.L04

1V_VGA_S0_PG
PWR_VGA_NVVDDS_PG

U7602 TC7SZ08FU-LJ-CT-GP

ALL_GPUPWGD

073.7SZ08.000G
2nd = 73.7SZ08.DAH
3rd = 73.01G08.L04

GFX_CLKREQ_CPU_N

084.00138.0A31
2nd = 84.05067.031

Q7601 PJA138KA-GP

R7603 10KR2J-3-GP

R7613 0R2J-2-GP

SYS_PEX_RST_MON_N

GPU_PEX_RST_N

GFX_CLKREQ_dGPU_N

GPU1A 1 OF 14
1/14 PCI_EXPRESS

	AG30	PEX_WAKE#
	AG29	PEX_RST#
	AG31	PEX_CLKREQ#
GFX_CLK_CPU_P	AE30	PEX_REFCLK
GFX_CLK_CPU_N	AE31	PEX_REFCLK*
GFX_PCIE_RX_P0	AC27	PEX_TX0
GFX_PCIE_RX_N0	AC28	PEX_TX0*
GFX_PCIE_TX_P0	AC30	PEX_RX0
GFX_PCIE_TX_N0	AC31	PEX_RX0*
GFX_PCIE_RX_P1	AA27	PEX_TX1
GFX_PCIE_RX_N1	AA28	PEX_TX1*
GFX_PCIE_TX_P1	AA31	PEX_RX1
GFX_PCIE_TX_N1	AA30	PEX_RX1*
GFX_PCIE_RX_P2	W27	PEX_TX2
GFX_PCIE_RX_N2	W28	PEX_TX2*
GFX_PCIE_TX_P2	W31	PEX_RX2
GFX_PCIE_TX_N2	W30	PEX_RX2*
GFX_PCIE_RX_P3	U28	PEX_TX3
GFX_PCIE_RX_N3	U27	PEX_TX3*
GFX_PCIE_TX_P3	U30	PEX_RX3
GFX_PCIE_TX_N3	U31	PEX_RX3*

PCIE/PLL DIGITAL PWR

PEX_DVDD_1	AA25
PEX_DVDD_2	U25
PEX_DVDD_3	V26
PEX_DVDD_4	W25
PEX_DVDD_5	Y25
PEX_DVDD_6	Y26
PEX_DVDD_7	

1V Interface

PEX_CVDD_1	AB25
PEX_CVDD_2	AB26

PCIE/PLL ANALOG PWR

PEX_HVDD_1	AC25
PEX_HVDD_2	AD25
PEX_HVDD_3	AE26
PEX_HVDD_4	AE27
PEX_HVDD_5	AE28
PEX_PLL_HVDD	AD26

1.8V Interface

OPS

PEX_CVDD_SENSE R30

PEX_TERMP R31 PEX_TERMP R7601 2K49R2F-GP

GN18-S5-GB3B-64-GP

071.0GN18.000U

1V_VGA_S0

1U 0402*4 X6S 4.7U 0603*1 X6S
1.713A Place near GPU

C7653 SC4D7U10V3KX-9-GP
C7629 SC1U10V2KX-18-GP
C7630 SC1U10V2KX-18-GP
C7631 SC1U10V2KX-18-GP
C7632 SC1U10V2KX-18-GP

10U 0805*2 X6S 22U 0805*1 X6S
Place between GPU and PS

C7624 SC10UD3V5KX-5DL-GP
C7623 SC10UD3V5KX-5DL-GP
C7636 SC22UD3V5KX-DL-GP

1U 0402*3 X6S
4.7U 0603*1 X6S
1.640A Place near GPU

1D8V_AON_S0

C7645 SC4D7U10V3KX-9-GP
C7633 SC1U10V2KX-18-GP
C7634 SC1U10V2KX-18-GP
C7635 SC1U10V2KX-18-GP

10U 0805*2 X6S 22U 0805*1 X6S
Place between GPU and PS

C7625 SC10UD3V5MX-DL-GP
C7626 SC10UD3V5MX-DL-GP
C7637 SC22UD3V5MX-1-DL-GP

1U 0402*1 X6S
Place near GPU
0.050A

1D8V_AON_S0

C7638 SC1U10V2KX-18-GP

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Title: GPU_960M_PEG (1/5)

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Date: Thursday, August 05, 2021 Sheet 76 of 106

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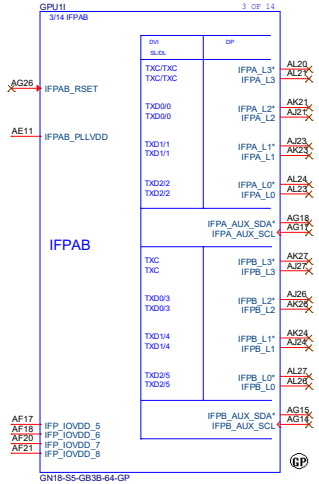

OPS

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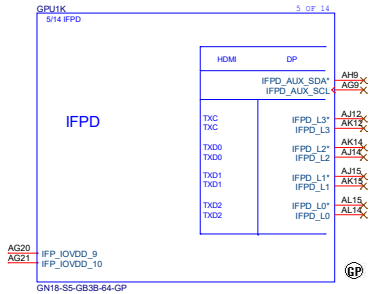

OPS

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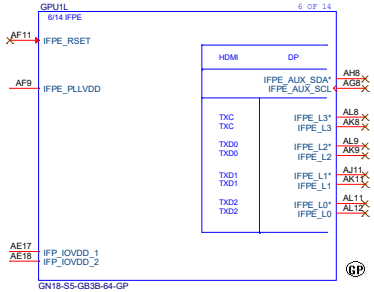

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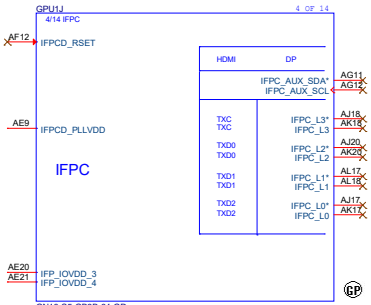

OPS

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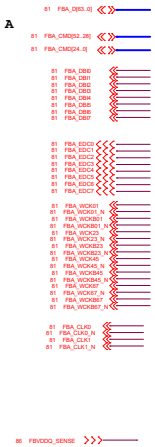
Group A

Group B



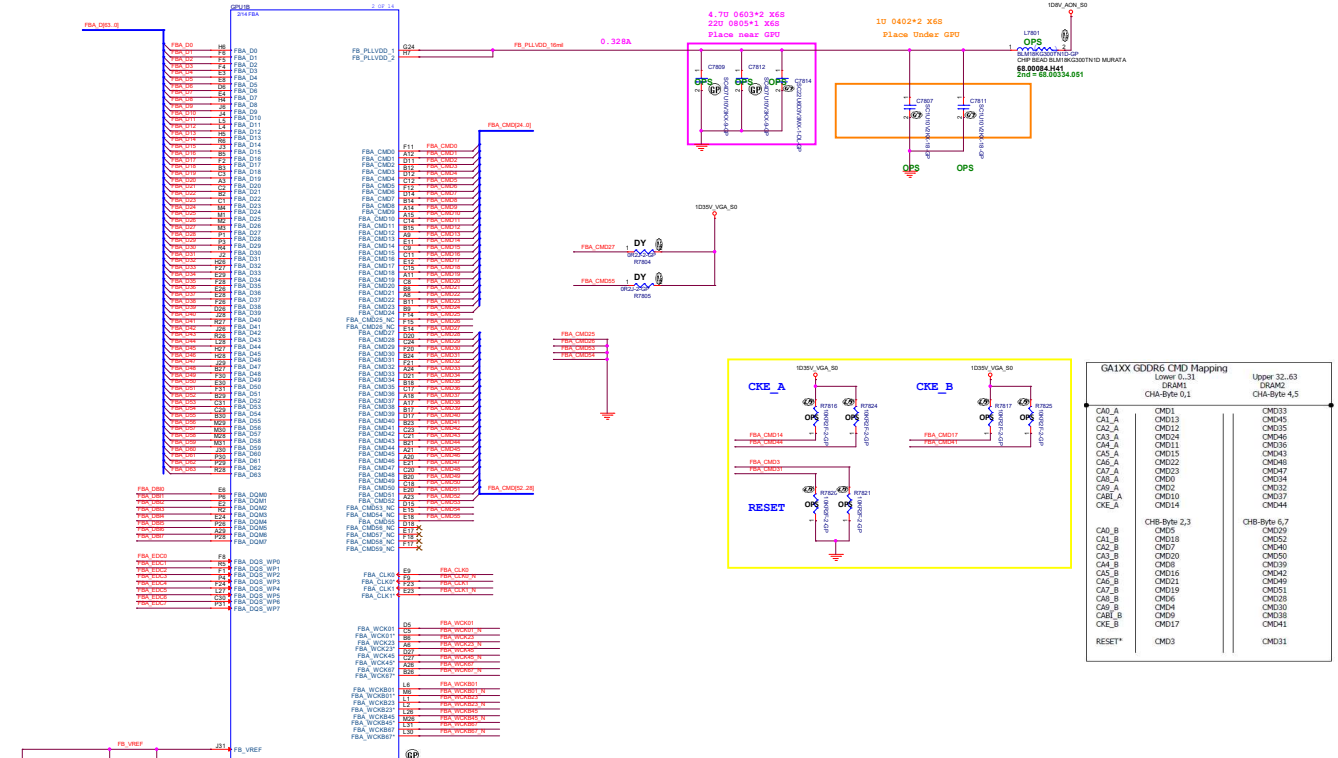
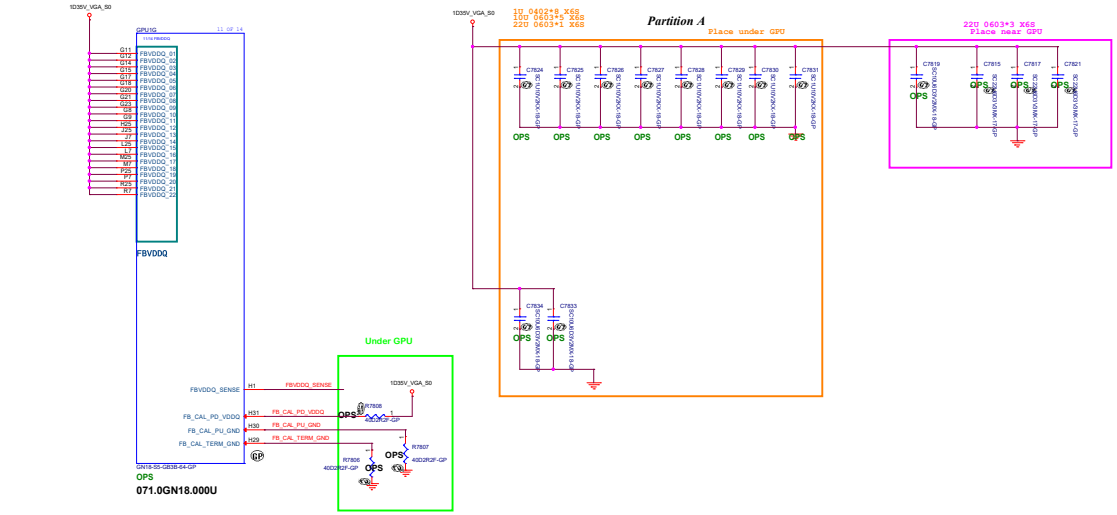


Table 4. GB3-64 and GB3B-64 FB BOM Differences

FB Pin	What to do for GB3-64	What to do for GB3B-64
FB_VREF	Pull down to 2.49 kΩ Refer to GB3-64 and GB3B-64 GPUs Co-Design Platform Development Package [PDP-JKQN-001]	Pull down to 49.9 ohm +3.9 pF Refer to GB3-64 and GB3B-64 GPUs Co-Design Platform Development Package [PDP-102N4-001]



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File: GPU_VRAM I/F (3/5)

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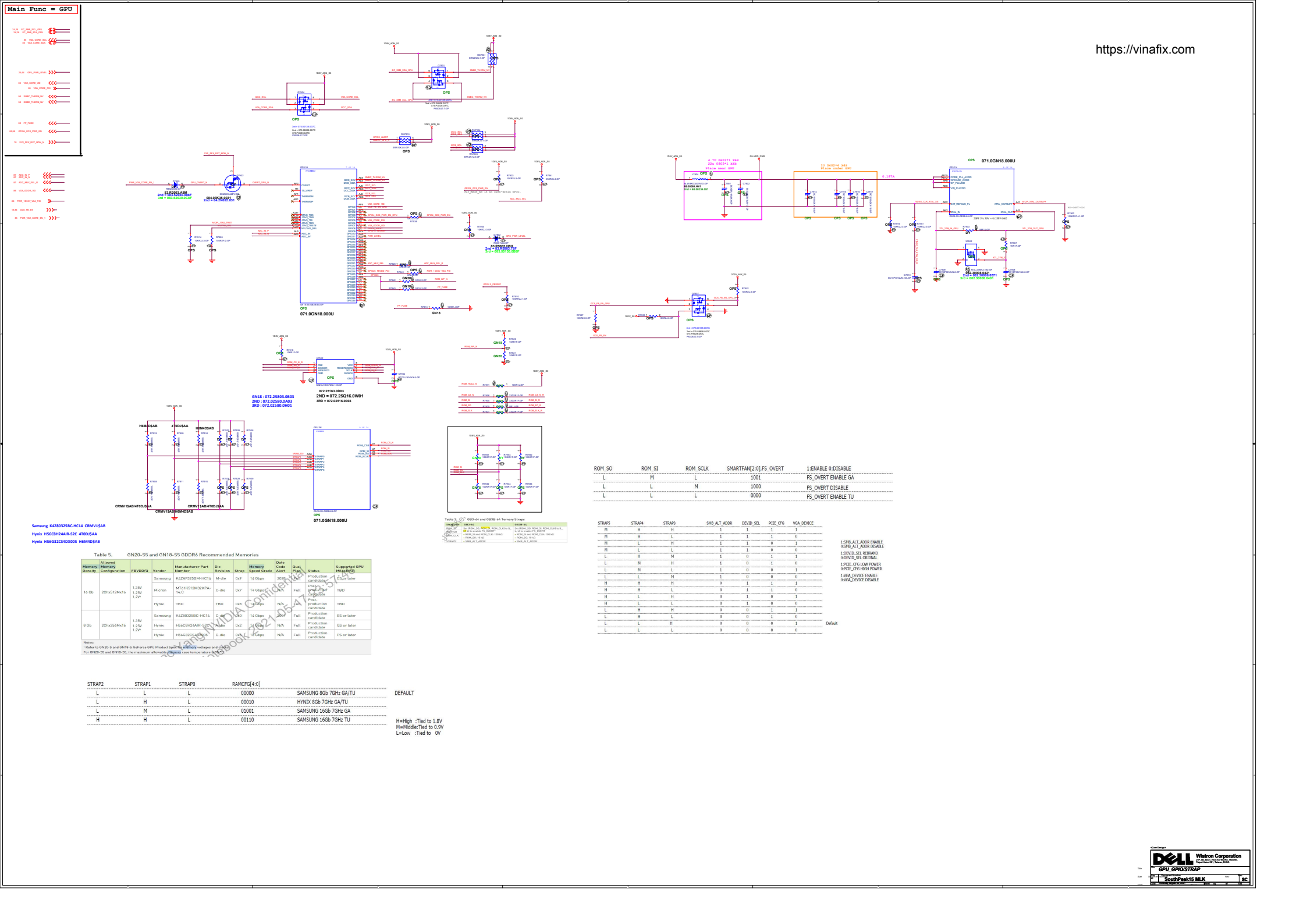

Table 5. GN20-S5 and GN18-S5 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC16	M-die	0x9	16 Gbps	2022	Full	Production candidate	ES or later
			Micron	MT61K512M32KPA-14:C	C-die	0x7	14 Gbps	N/A	Full	Pre/Post-production candidate	TBD
			Hynix	TBD	TBD	0x8	16 Gbps	N/A	Full	Post-production candidate	TBD
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZB80325BC-HC16	C-die	0x0	16 Gbps	2044	Full	Production candidate	ES or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	QS or later
			Hynix	H5AG32C54DX005	C-die	0x5	16 Gbps	N/A	Full	Production candidate	PS or later

Notes:
[1] Refer to GN20-S and GN18-S GeForce GPU Product Spec for memory voltages and clocks.
For GN20-S5 and GN18-S5, the maximum allowable memory case temperature is 95°C.

Table 3. GB3-64 and GB3B-64 Ternary Straps

Strap Pin	GB3-64	GB3B-64
ROM_SO	Sel ROM_SO, ROM_SI, ROM_CLK) to 0, 1, or 2 to enable FS_OVERT	Sel ROM_SO, ROM_SI, ROM_CLK) to 0, 1, or 2 to enable FS_OVERT
ROM_SI	= ROM_SI and ROM_CLK= 100 kΩ	= ROM_SI and ROM_CLK= 100 kΩ
ROM_CLK	= ROM_SO: 10 kΩ	= ROM_SO: 10 kΩ
STRAP5	= SHB_ALT_ADDR	= SHB_ALT_ADDR

Main Func = GPU

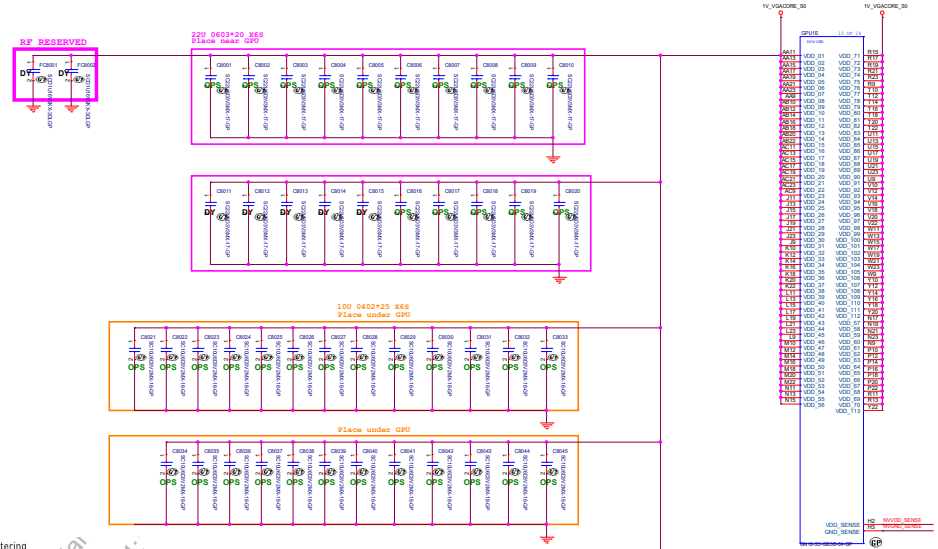

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Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU			Filtering near GPU		
			Footprint	BOM[1]	Value[2]	Footprint	BOM[1]	Value[2]
NVVDD + MSVDD (merged)	113	Varies	8 25	8 25	1uF 10uF	20 3	15 3	22uF 330uF
FBVDDQ (GPU side)[1,3]	22	1.20V / 1.25V / 1.35V	8 2	8 2	1uF 10uF	1 3	1 3	10uF 22uF
FB_PLLVDD	2	1.8V	2	2	1uF (1 per ball)	1 1 2	1 1 2	30D bead 22uF 4.7uF
CORE_PLL_AVDD GPCPLL_AVDD SP_PLLVDD VID_PLLVDD IFPAB_PLLVDD IFPCD_PLLVDD IFPE_PLLVDD	1 1 1 1 1 1 1	1.8V	7	7	1uF (1 per ball)	1 1 1	1 1 1	30D bead 22uF 4.7uF
IFP_IOVDD	10	0.95V	8	8	1uF	3 3	3 3	4.7uF 1uF
PEX_DVDD	7	0.95V	4	4	1uF	2	2	10uF
PEX_CVDD	2		1	1	4.7uF	1	1	22uF
PEX_HVDD	2	1.8V	3	3	1uF	2	2	10uF
PEX_PLL_HVDD	1		1	1	4.7uF	1	1	22uF
1V8	4	1.8V	4	4	1uF	3 3	3 3	1uF 4.7uF

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GPU_POWER/GND (5/5)

SouthPeak15 MLK

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Tuesday, August 03, 2021

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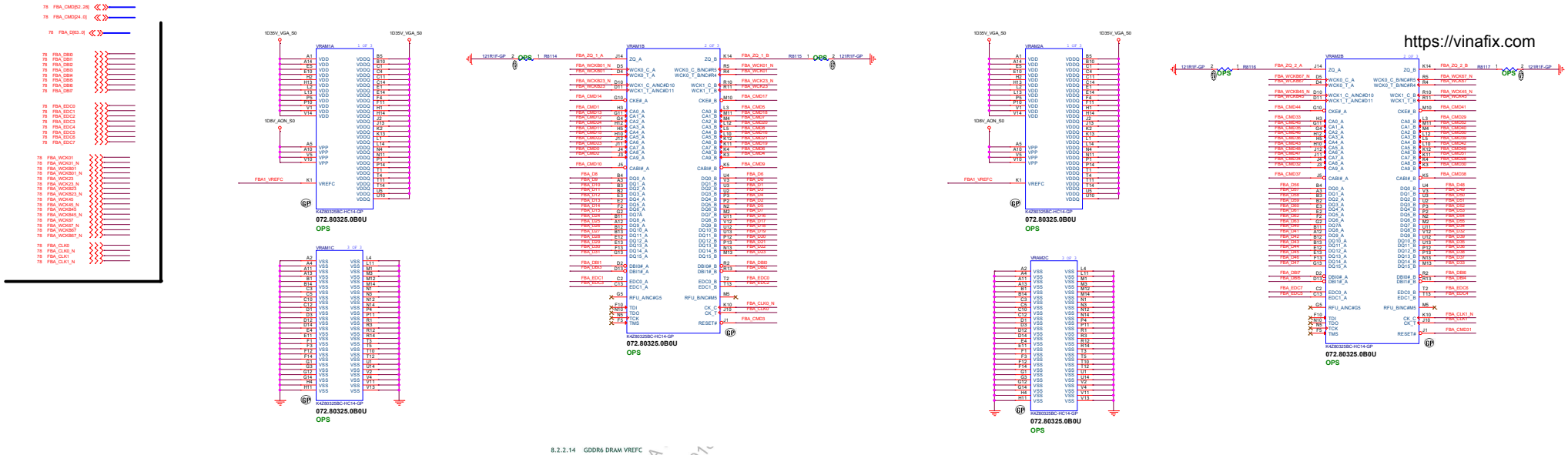

8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 8.8 illustrates use of the integrated VREFC for ×16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

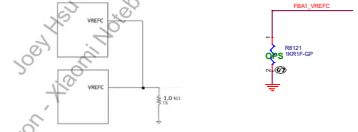

Figure 8.8 Use of Integrated VREFC for ×16 Mode

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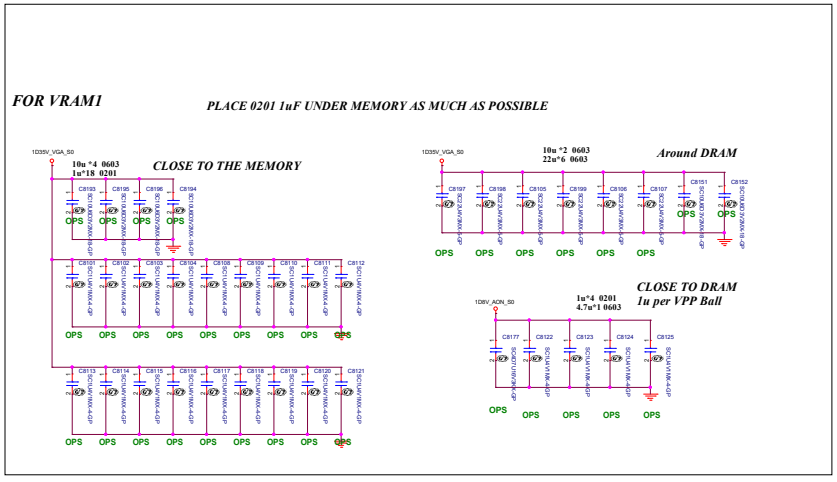

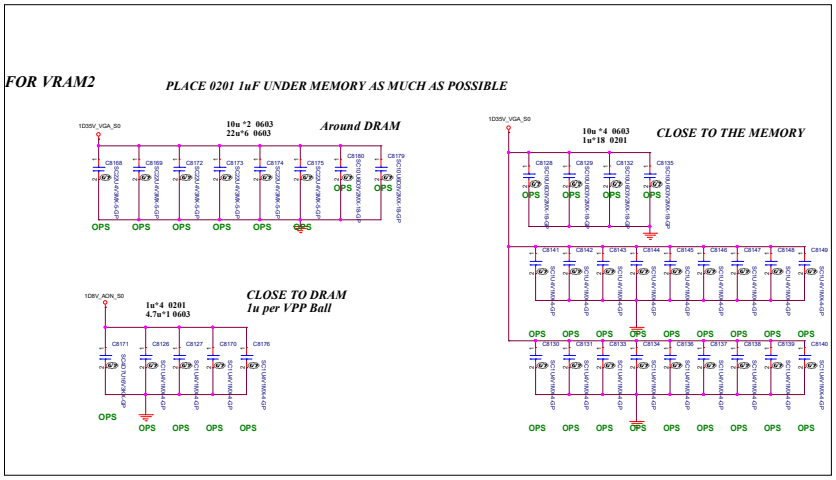

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Date: Thursday, August 05, 2021 Sheet 83 of 106

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Title: *VGA Power B*

Size	Document Number	Rev
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OFFPAGE-Signal

OFFPAGE-GAP

MP2988 For NVVDDS

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80 NVVDD_SENSE — PR8542 0R2J-2-GP — PWR_VGA_CORE_VSP

80 NVGND_SENSE — PR8543 0R2J-2-GP — PWR_VGA_CORE_VSN

76,86 PWR_VGA_NVDDDS_PG — PR8544 0R2J-2-GP — PWR_VGA_CORE3_PG

EE need check

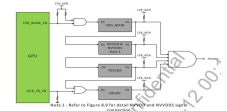

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

76,86 1V_VGA_S0_PG — PR8531 0R2J-2-GP — DGPU_PWROK_L — U8502 TC7SZ08FU(TE12L,F) — 3D3V_S0

80 PWR_1D35V_VGA_PG — PR8532 0R2J-2-GP — 1D35V_PGOOD_L — DGPU_PWROK 6,24

073.7S208.800G
2nd = 73.7S208.12A1
3rd = 73.01G08.L04

For VGA_CORE sequence
EE need check

79,86 GPIO4_GC6_PWR_EN — R8541 10KR2J-3-GP — Q8509 PJT138KA-GP — PWR_VGA_NVVDD_OR# — 1V_VGA_EN_R 86

C8502 SCD22U10V1KX-1-GP

075.00138.0A7C
2nd = 075.00139.007C
3rd = 075.00138.0F7C

1D8V_AON_S0 — R8529 10KR2J-3-GP — Q8504 2N7002K-2-GP-U — PWR_VGA_NVVDD_OR# — PWR_VGA_CORE_EN — R8501 470R2F-GP — PWR_VGA_CORE_EN_1 79

C8501 SC1U16V2KX-3DLGP

84.2N702.J31
2ND = 084.27002.0N31
3rd = 084.27002.0L31
4th = 084.27002.0K31

PG Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWM/VID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh

PMBus Address	Setting Point(V)	R_{SGAIN} (kΩ) 1%	R_{SOFS} (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

3D3V_S5 — 1D8V_AON_S0 — PR8552 10KR2F-2-GP — PR8553 10KR2F-2-GP — PR8551 4K99R2F-L-GP — PR8550 5K09R2F-L-GP — PR8554 10KR2F-2-GP — PR8555 10KR2F-2-GP

PWR_VGA_CORE_EN_1 — PR8535 0R2J-2-GP

79 VGA_CORE_PSI — PR8523 0R2J-2-GP — PR8524 10KR2F-2-GP

79 VGA_CORE_SCL — PR8587 0R2J-2-GP

79 VGA_CORE_SDA — PR8519 0R2J-2-GP

79 VGA_CORE_VID — PR8522 0R2J-2-GP — PR8558 10KR2F-2-GP

PWR_NVVDD_SCL — PWR_NVVDD_SDA — PWR_NVVDD_PSI — PWR_NVVDD_EN — PWR_VGA_CORE3_PG — PWR_NVVDD_PWM0

PU8501 MP2988GQ-1059-Z-GP

074.02988.M004

FW update : 074.02988.M004

PWR_NVVDD_DRMOS_VTEMP — PR8557 0R2J-2-GP — PC8524 SC1U10V2KX-1DLGP — PWR_NVVDD_VDD18 — PWR_NVVDD_VTEMP — PR8556 49K9R2F-L-GP — PC8519 SC1U25V3KX-1DLGP

PR8561 100R2F-L1-GP-U — PC8501 SCD1U25V2KX-1-DL-GP — PWR_VGA_CORE_VSN — PWR_VGA_CORE_VSP — 1V_VGACORE_S0 — PR8562 100R2F-L1-GP-U

PWR_DCBATOUT_NVVDD — PR8571 2M49R2F-GP — PWR_NVVDD_VINSEN — PR8570 133KR2F-GP — PC8525 SCD01U25V2KX-3DLGP — PR8574 1KR2F-3-GP — PR8575 1KR2F-3-GP — PWR_NVVDD_CS_PH2 — PWR_NVVDD_CS_PH1

PWR_DCBATOUT_NVVDD — PD8501 MMSD4148-2DL-R7G-GP — 083.04024.0AA1 2nd = 83.PJSD2.0AF

1V_VGACORE_S0 — PC8501 SC1U16V2KX-1DLGP — PC8502 SC330U2VM-5-GP — PC8503 SC330U2VM-5-GP — PC8504 SC1U25V2KX-4-GP — PC8505 SC1U25V2KX-4-GP — PC8506 SC1U25V2KX-4-GP — PC8507 SC1U25V2KX-4-GP — PC8508 SC1U25V2KX-4-GP

1V_VGACORE_S0 — PC8509 SC330U2VM-5-GP — PC8510 SC330U2VM-5-GP — PC8511 SC1U25V2KX-4-GP — PC8512 SC1U25V2KX-4-GP — PC8513 SC1U25V2KX-4-GP — PC8514 SC1U25V2KX-4-GP — PC8515 SC1U25V2KX-4-GP

GN20/GN18-S5
EDP:31A
EDP-Peak:100A

3D3V_S5 — PR8576 2KR2F-3-GP — PU8502 MP86941-CGQVT-Z-GP — PWR_NVVDD_PWM1 — PWR_NVVDD_VRMODE_VTEMP — PWR_NVVDD_CS_PH1 — PR8577 0R2J-2-GP — PR8578 0R2J-2-GP — PR8579 0R2J-2-GP — PWR_NVVDD_PWM_PH1 — PWR_NVVDD_VTEMP1 — PWR_NVVDD_SYNC1 — PWR_NVVDD_CS1

074.86941.M008
2ND = 074.86941.M010

Close to PU8502

PC8526 SC1U25V2KX-4-GP — PC8527 SC1U10V2KX-1DLGP — PWR_NVVDD_BST1 — PWR_NVVDD_SW1 — PL8501 IND-D1305-R8-GP — 7.1mmx7.6mmx3.0mm DCR: 0.72mohm +/-5% Idc : 40A , Isat : 60A — 068.R1510.2421 2nd = 068.R1510.1511 — PR8539 2R2R3F-2-GP — PWR_NVVDD_SN_PH1 — PC8547 SC1KP50V2KX-1DLGP

PWR_NVVDD_PWM2 — PWR_NVVDD_VRMODE_VTEMP — PWR_NVVDD_CS_PH2 — PR8577 2KR2F-3-GP — PR8578 0R2J-2-GP — PR8579 0R2J-2-GP — PWR_NVVDD_PWM_PH2 — PWR_NVVDD_VTEMP2 — PWR_NVVDD_SYNC2 — PWR_NVVDD_CS2

074.86941.M008
2ND = 074.86941.M010

Close to PU8503

PC8528 SC1U25V3KX-1-DLGP — PWR_NVVDD_BST2 — PWR_NVVDD_SW2 — PL8502 IND-D1305-R8-GP — 7.1mmx7.6mmx3.0mm DCR: 0.72mohm +/-5% Idc : 40A , Isat : 60A — 068.R1510.2421 2nd = 068.R1510.1511 — PR8580 2R2R3F-2-GP — PWR_NVVDD_SN_PH2 — PC8548 SC1KP50V2KX-1DLGP

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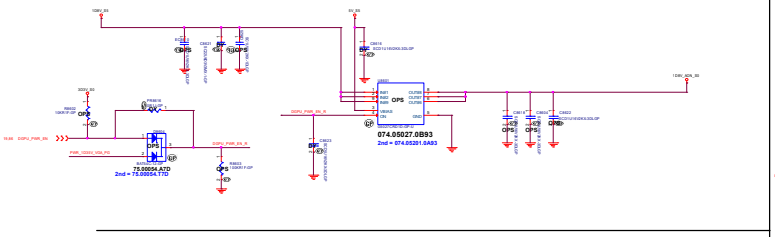
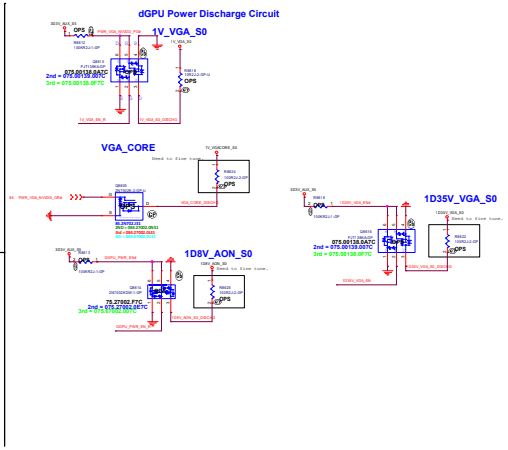
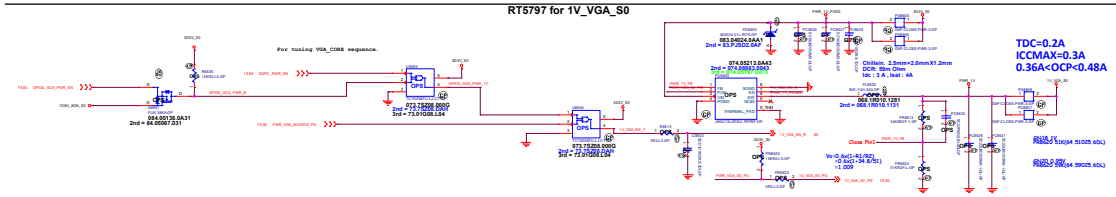
AOZ2260 For VGA 1D8V



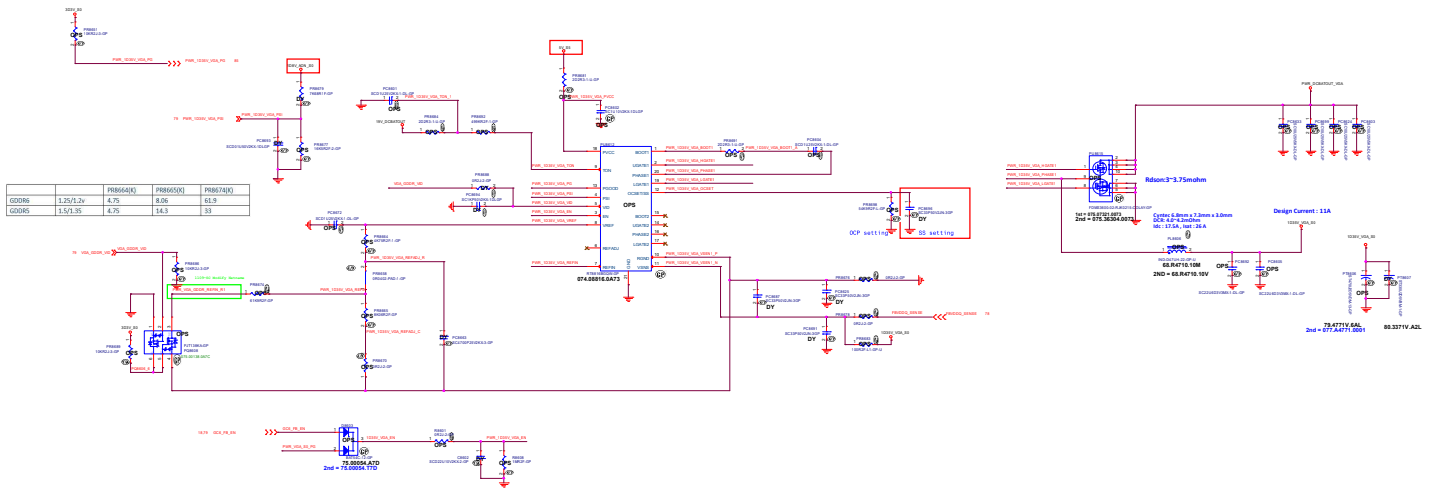
1D8V_AON_S0 to 1D8V_VGA_S0



RT5797 for 1V_VGA_S0



RT8816B for 1D35V_VGA_S0



		P88664(K)	P88665(K)	P88674(K)
GDDR6	1.25/1.2v	4.75	8.06	61.9
GDDR5	1.5/1.35	4.75	14.3	33

OVR-M Gen1

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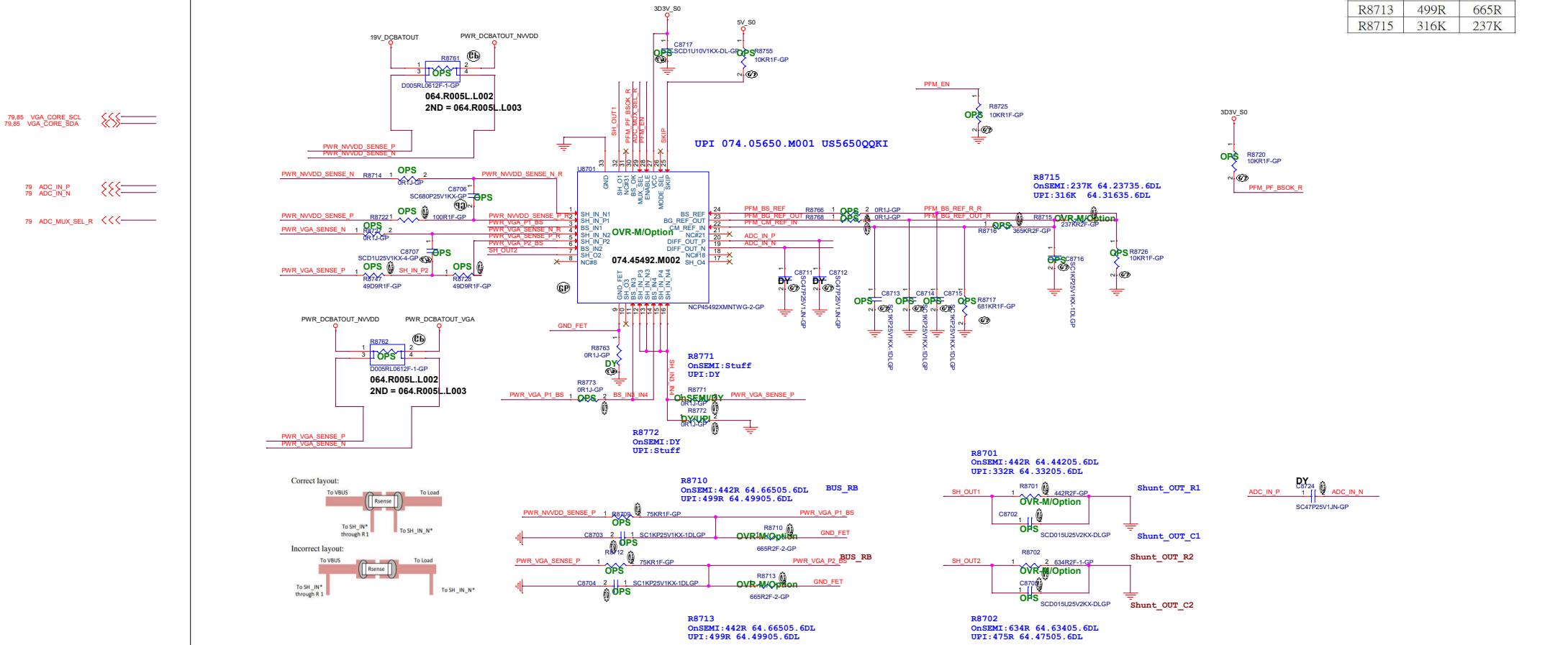
	uP1	OnSEMI
R8771	DY	Stuff
R8772	Stuff	DY
R8701	332R	442R
R8702	475R	634R
R8710	499R	665R
R8713	499R	665R
R8715	316K	237K



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Title: Discharge

Size: A2 | Document Number: SouthPeak15 MLK | Rev: SC

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Title

Reserved

Size	Document Number	Rev
A4	Odin ADL-P	SC

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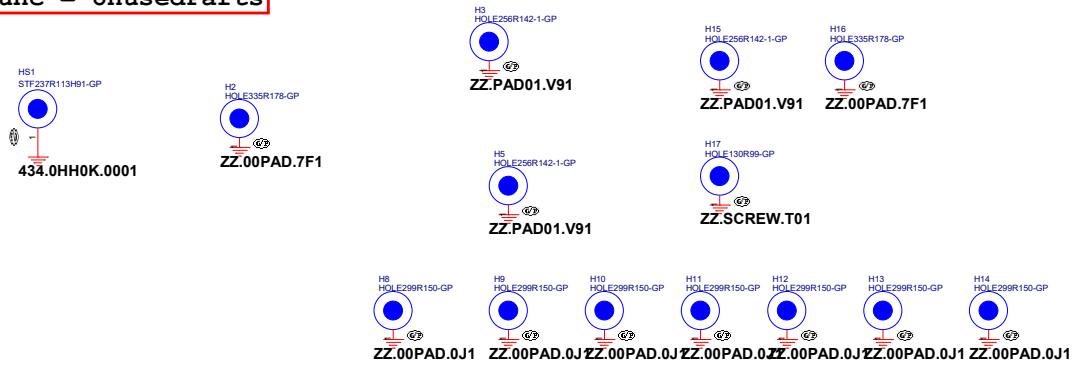
Main Func = UnusedParts



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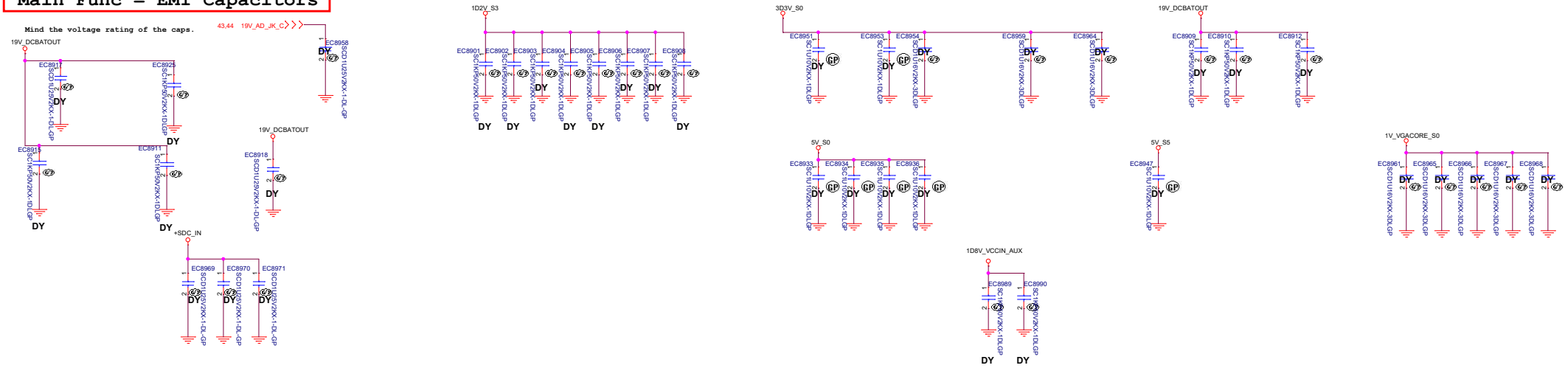
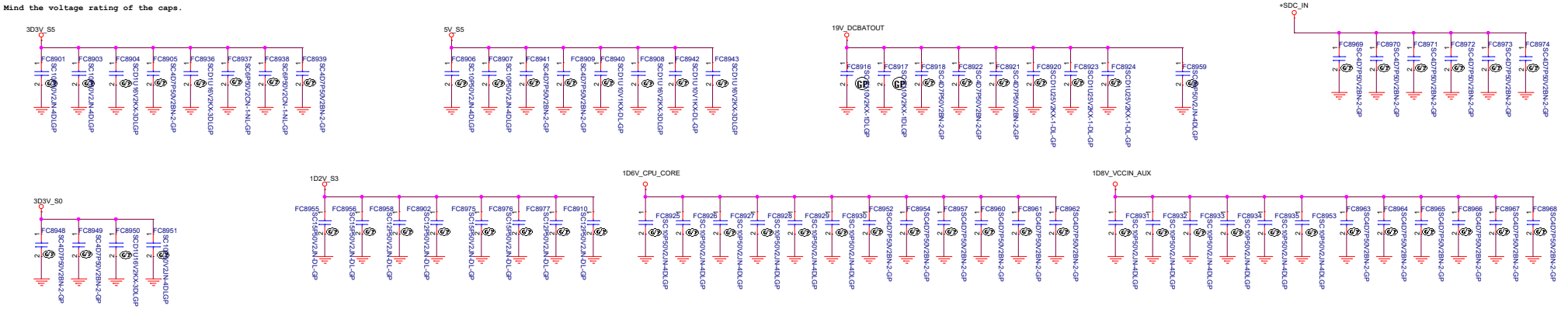
Main Func = EMI Capacitors

Mind the voltage rating of the caps.



Main Func = RF Capacitors

Mind the voltage rating of the caps.



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Title: UNUSED PARTS/EMI Capacitors

Size: A2 | Document Number: Odin ADL-P | Rev: SC

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Title

Reserved

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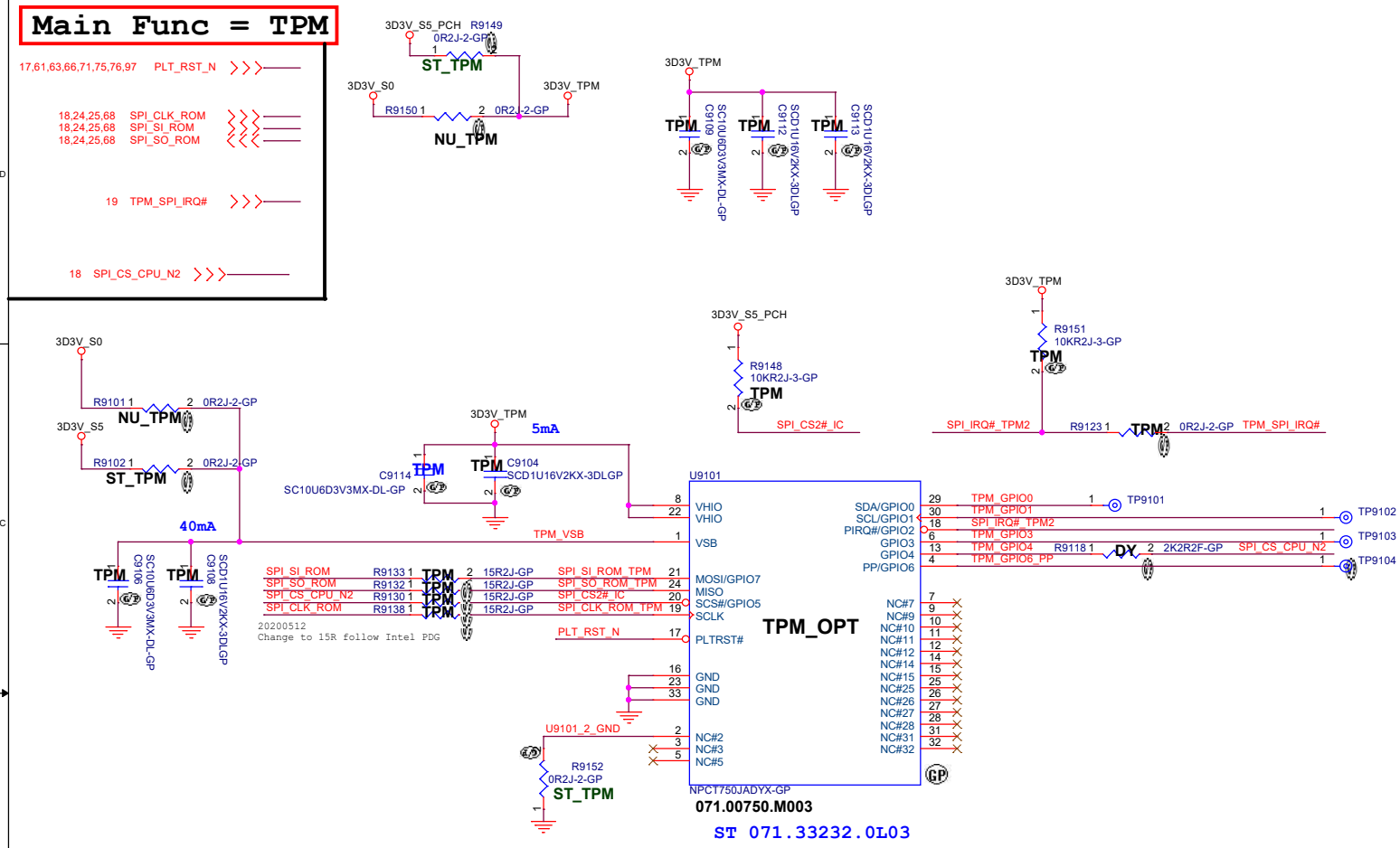
Main Func = TPM



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Title: INT IO (TPM)

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SSID = Finger Print

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Title: ***Finger Print***

Size	Document Number	Rev
A4	***Odin ADL-P***	***SC***

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Title: *(Reserved)*

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Title: *(Reserved)*

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Title: *(Reserved)*

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Main Func = (R360)SIV Auto Test_SI Test point

SIV Auto Test

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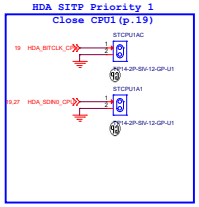
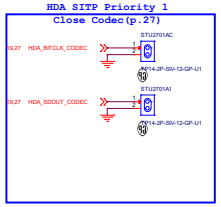
HDA SITP Priority 1
Close CPU1(p.19)



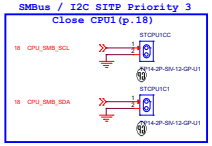
HDA SITP Priority 1
Close Codec(p.27)



ESPI SITP Priority 2
Close CPU(p.18)

ESPI SITP Priority 2
Close EC(p.24)

SMBus / I2C SITP Priority 3
Close CPU1(p.18)

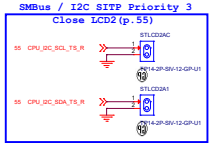


SMBus / I2C SITP Priority 3
Close CPU1(p.20)

SMBus / I2C SITP Priority 3
Close U2401(p.24)

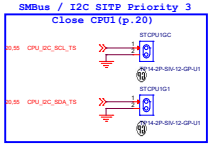
SMBus / I2C SITP Priority 3
Close BATT1(p.43)

SMBus / I2C SITP Priority 3
Close LCD2(p.55)

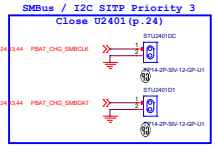


SMBus / I2C SITP Priority 3
Close CPU1(p.18)

SMBus / I2C SITP Priority 3
Close CPU1(p.20)

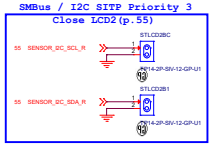


SMBus / I2C SITP Priority 3
Close U2401(p.24)



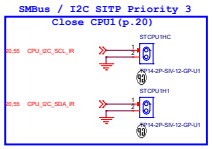
SMBus / I2C SITP Priority 3
Close PD4401(p.44)

SMBus / I2C SITP Priority 3
Close LCD2(p.55)



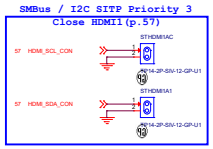
SMBus / I2C SITP Priority 3
Close CPU1(p.18)

SMBus / I2C SITP Priority 3
Close CPU1(p.20)

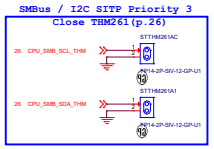


SMBus / I2C SITP Priority 3
Close U2401(p.24)

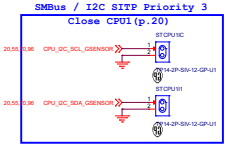
SMBus / I2C SITP Priority 3
Close HDMI1(p.57)



SMBus / I2C SITP Priority 3
Close THM261(p.26)



SMBus / I2C SITP Priority 3
Close CPU1(p.20)

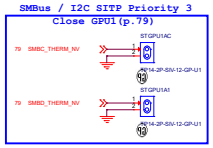


SMBus / I2C SITP Priority 3
Close U2401(p.24)

SMBus / I2C SITP Priority 3
Close TP1(p.65)

SMBus / I2C SITP Priority 3
Close SSD1(p.63)

SMBus / I2C SITP Priority 3
Close GPU1(p.79)



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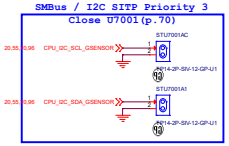
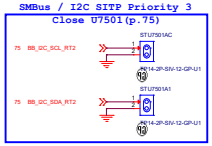
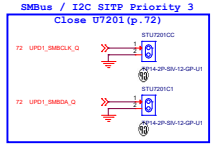
Close U7001(p.70)



SMBus / I2C SITP Priority 3
Close U7501(p.75)

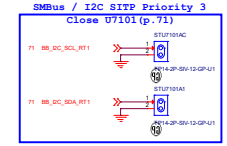


SMBus / I2C SITP Priority 3
Close U7201(p.72)

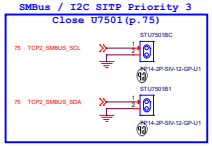


SMBus / I2C SITP Priority 3
Close DM1(p.12)

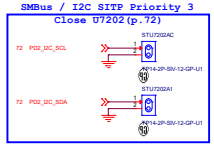
SMBus / I2C SITP Priority 3
Close U7101(p.71)



SMBus / I2C SITP Priority 3
Close U7501(p.75)

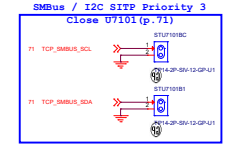


SMBus / I2C SITP Priority 3
Close U7202(p.72)



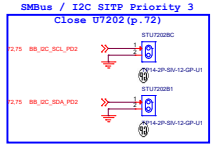
SMBus / I2C SITP Priority 3
Close DM2(p.13)

SMBus / I2C SITP Priority 3
Close U7101(p.71)



SMBus / I2C SITP Priority 3
Close U7201(p.72)

SMBus / I2C SITP Priority 3
Close U7202(p.72)



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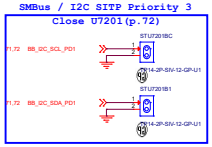
Close U7201(p.72)



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Title: SITP

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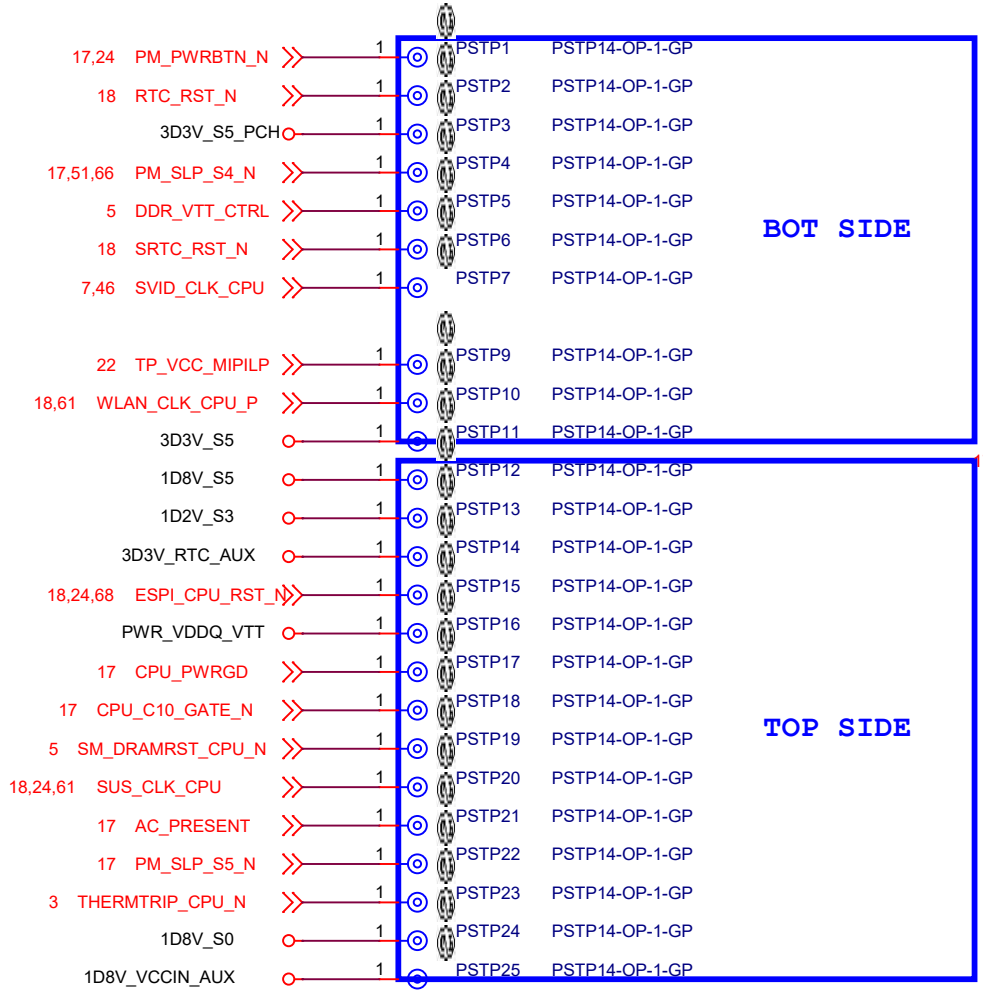

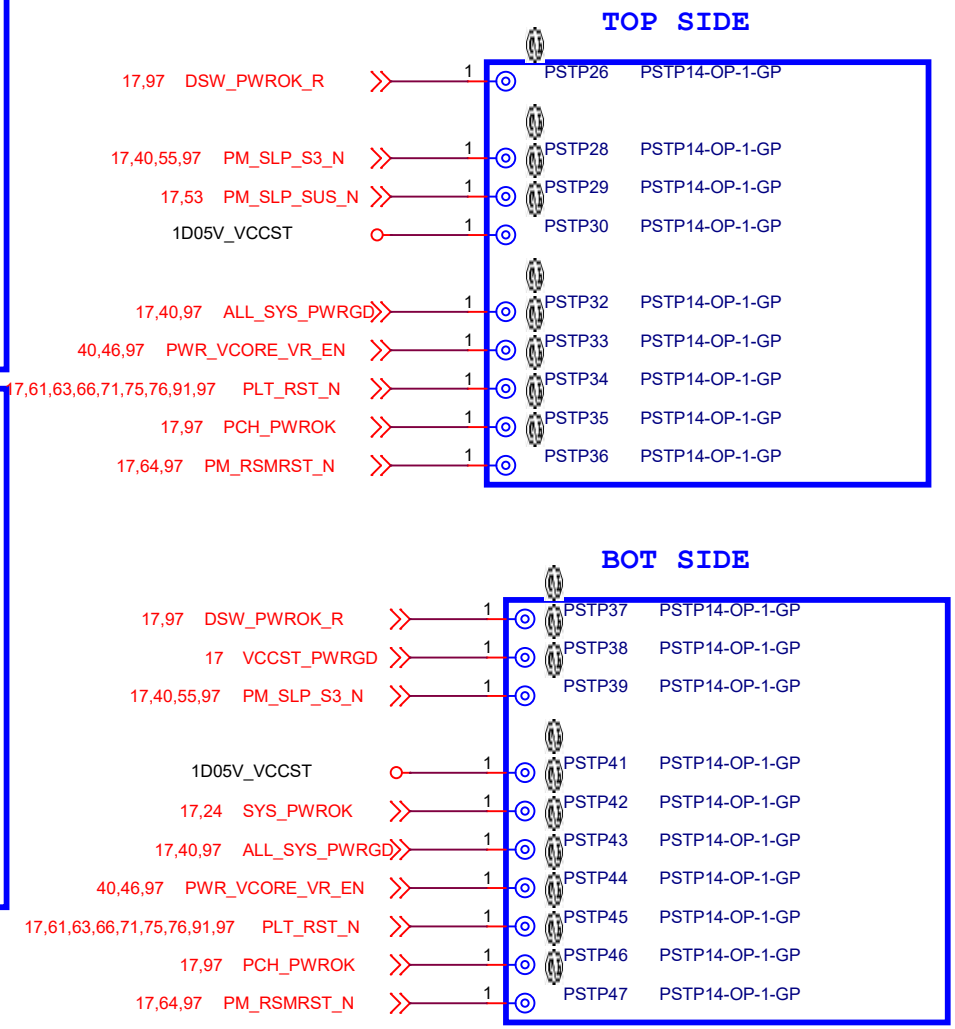

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Title: PSTP

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Main Func = Firmware SW

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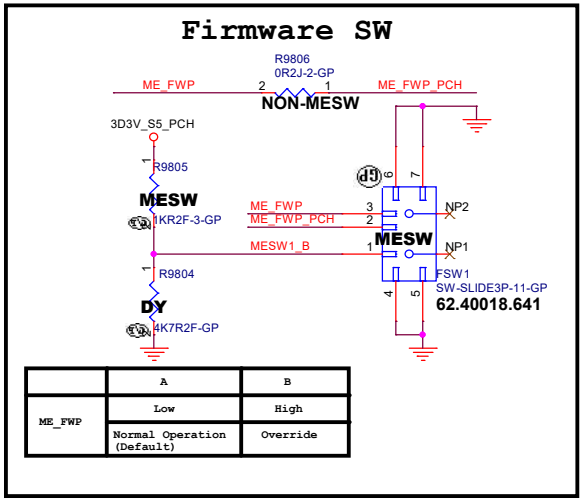
15 ME_FWP_PCH
24 ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

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Title: CRT_Switch

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Title

Debug (XDP debug)

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CLK Block Diagram

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TBD

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Title: CLK Block Diagram

Size	Document Number	Rev
A2	Odin ADL-P	SC

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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: *Change History*

Size	Document Number	Rev
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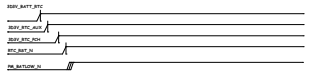
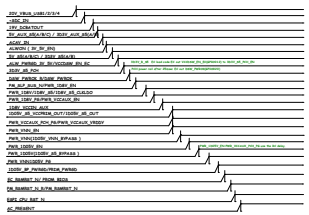
POWER UP SEQUENCE

G3 to S5 [Non-Deep Sx Platform]

(RTC)

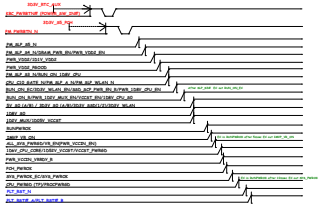


(TypeC Adapter Pull-in)

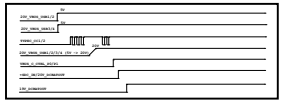


S5 to S0 [Non-Deep/Deep Sx Platform]

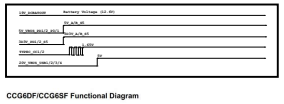
(Power Button On)



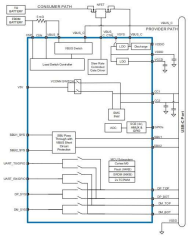
Type-C Adapter IN sequence 20V



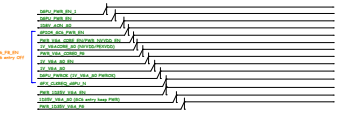
Type-C Charger out sequence 5V

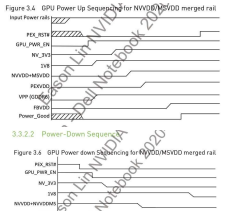


CCG6DF/CCG6SF Functional Diagram

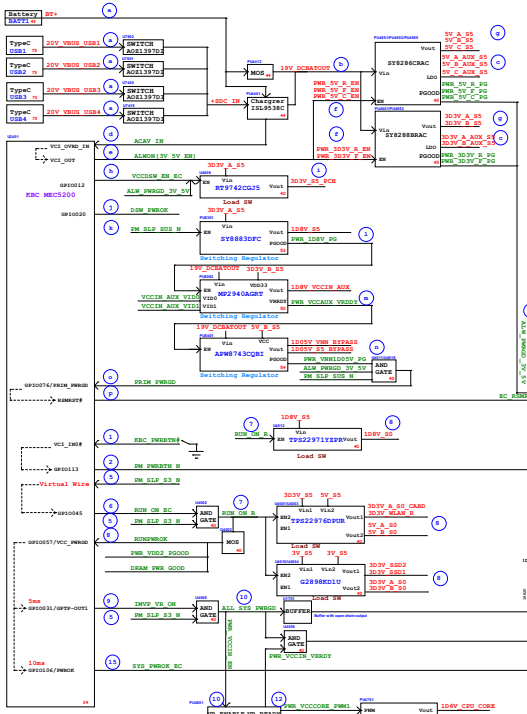


GPU POWER UP SEQUENCE





POWER UP SEQUENCE DIAGRAM



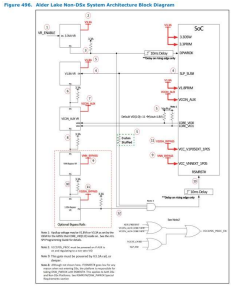


Figure 499. PWROK Generation Flow Diagram

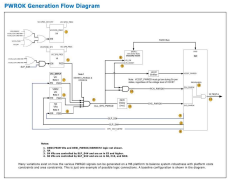
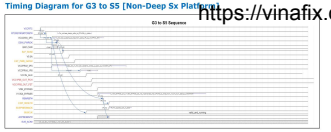


Figure 502. Timing Diagram for G3 to S5 [Non-Deep Sx Platform]



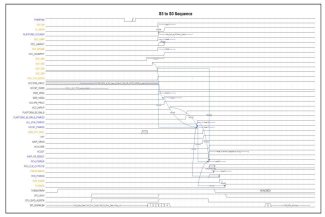


Figure 506. Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]

For S0 to G3 Sequence 1 of 2 Refer to DSx Sequence

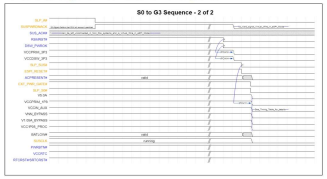
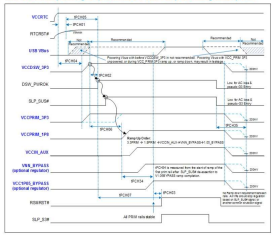


Figure 510. Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



(Discrete only) POWER UP SEQUENCE DIAGRAM

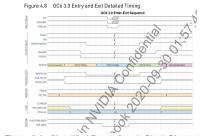
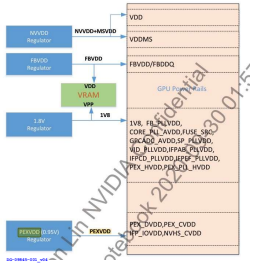
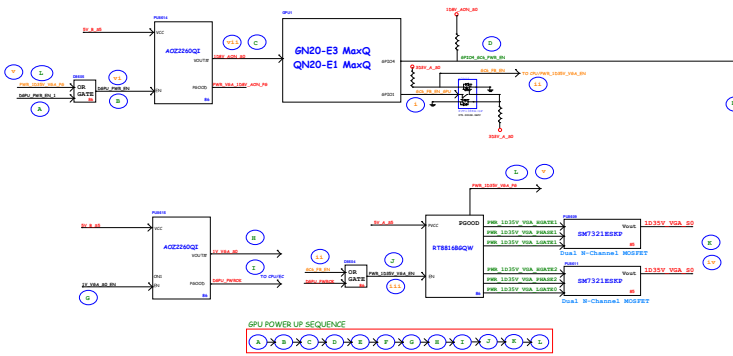


Figure 3.1 Simplified Power Supply Block Diagram





GPU POWER UP SEQUENCE

GC6 3.0 entry

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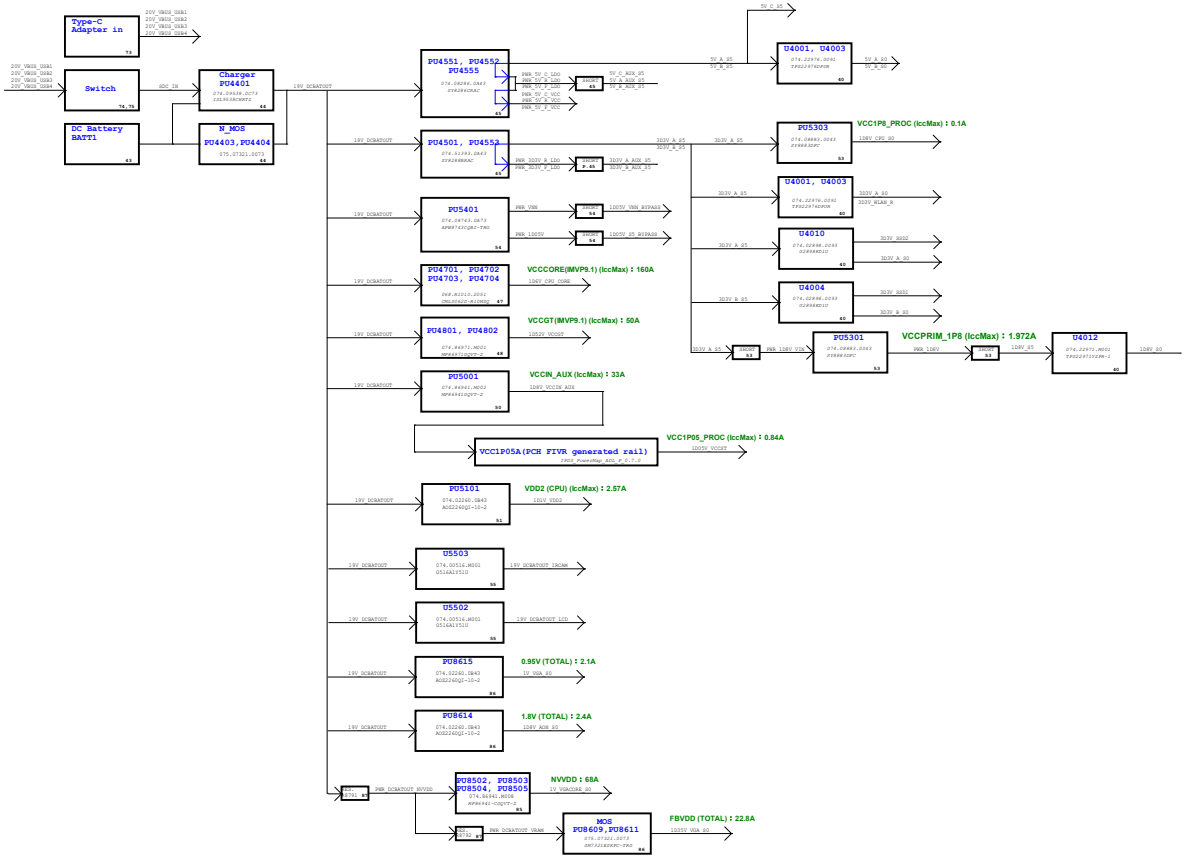
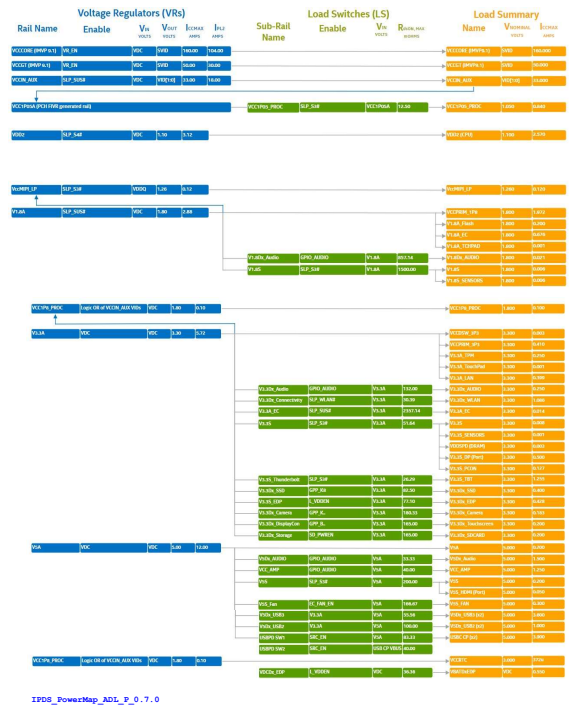
POWER BLOCK DIAGRAM





IPDS_PowerMap_ADL_P_0.7.0

7.1 Power and Ground Signals

This section describes the PCH power rails.

Table 12. Power and Ground Signals

Name	Description
VCCIN_AUX	FIVR Input rail: 1.8 V
VCC_VNNEXT_1P05	Used for FIVR PRIM_CORE bypass mode during S0ix and Sx: 1.05 V
VCC_V1P05EXT_1P05	Used for FIVR PCH IO bypass mode during S0ix and Sx: 1.05 V
VCCA_CLKLDO_1P8	Analog supply for internal clocks: 1.8 V
VCCPRIM1P05_OUT_PCH	1.05 V Primary Well: for CNVi and other internal I/O blocks.
VCCDSW_1P05	Deep Sx Well: 1.05 V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.
VCCPRIM_1P8	1.8 V Primary Well.
VCCPRIM_3P3	3.3 V Primary Well.
VCCPGPPR	Audio Power 3.3 V or 1.8 V. If powered at 3.3 V, the 3.3 V supply can come from VCCPRIM_3P3 supply. If powered at 1.8 V, the 1.8 V supply can come from VCCPRIM_1P8 supply.
VCCDSW_3P3	3.3 V Deep Sx Well.
VCCRTC	RTC Well Supply. This rail can drop to 2.0 V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. *Notes:* 1. VCCRTC nominal voltage is 3.0 V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. 2. Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VCCDPHY_1P24	1.24 V for CNVi logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide (PDG) for implementation details.
VCCLDOSTD_OP8S	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose.
VCC1P05_OUT_FET	FIVR output rail: 1.05 V, used for CPU rails VCCST/STG.

continued...

11.12 Processor Power Rails

Table 73. Processor Power Rails Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
VCCCORE	Processor IA Cores and Ring power rail	I	PWR	–	S Processor Line P Processor Line
VCCGT	Processor Graphics power rail	I	PWR	–	S Processor Line P Processor Line
VCCIN_AUX	Support internal FIVR's, SA, PCIe, Display SO and other internal Blocks.	I	PWR	–	S Processor Line P Processor Line
VCCIN_AUX_FLTR	Support internal FIVR's, SA, PCIe, Display DO and other internal Blocks. this pin should be shorted on the platform to VCCIN_AUX power rail	I	PWR	–	S Processor Line P Processor Line
VCC1P05_PROC	Sustain and Sustain Gated Power Rail	I	PWR	–	S Processor Line P Processor Line
VCC1P8_PROC	PCIE PHY Power 1.8V Rail	I	PWR	–	S Processor Line P Processor Line
VDD2	System Memory power rail	I	PWR	–	S Processor Line P Processor Line
VDD2_EDGECAP	Internal power pin, this pin should be connected to a decoupling capacitor and ground	I		–	S Processor Line
VCCIN_AUX_EDGECAP	Internal power pin, this pin should be connected to a decoupling capacitor and ground	I		–	S Processor Line
VDD2_DDRS_SENSE	Isolated, low impedance DDRS voltage sense pins.	N/A	PWR SENSE	–	S Processor Line P Processor Line
VCCGT_SENSE VCC_SENSE VCCIN_AUX_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	PWR SENSE	–	S Processor Line P Processor Line S Processor Line P Processor Line
VCC1P05_PROC_SENSE					S Processor Line
VCC1P05_OUT					P Processor Line
VCC_DESPRO					P Processor Line
VCC_MILP					P Processor Line

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
VCC_CFG_PU_OUT	Configuration Signals: Refer to the appropriate platform design guide for pull-up recommendations when a logic low is desired	I	GTL	SE	P/S Processor Line

Table 11. Output EDP-c Specifications

	TGP	NVVDD	FB TOTAL	0.95V Total[1]	1.8V Total[2]
	(W)	(A)	(A)	(A)	(A)
GN20-E7	95	115	39	2.1	2.9
	105	123	39	2.1	2.9
	135	123	39	2.1	2.9
	145	123	44	2.1	2.9
	150	123	44	2.1	2.9
GN20-E7 Max-Q	80	89	25	2	2.4
	90	98	25	2	2.4
GN20-E5	115	108	45	2.1	2.9
	125	116	45	2.1	2.9
GN20-E5 Max-Q	80	83	32	2	2.4
	90	93	32	2	2.4

	TGP	NVVDD	FB TOTAL	0.95V Total[1]	1.8V Total[2]
	(W)	(A)	(A)	(A)	(A)
GN20-E3	80	81	25	2.1	2.9
	90	90	25	2.1	2.9
	100	97	25	2.1	2.9
	115	109	25	2.1	2.9
GN20-E3 Max-Q	60	66	20	2	2.4
	70	75	20	2	2.4

Notes:
[1] 0.95V Total includes the PCIe and other 0.95V rails except the IFP_IOVDD rail. Add 305 mA for each IFP in use for DP/HDMI.
[2] 1.8V Total includes all PLL, PCIe, 1V8, and other 1.8V rails except the IFPx_PLLVDD power rail. Add 330 mA for each IFP in use.
[3] Power supply rail voltages set to maximum DC tolerance. Worst case current is observed at GPU maximum operating temperature.
[4] FB TOTAL EDPc current is the total of FBVDD+FBVDDQ, which includes GPU and memory EDPc current. These values are with nominal memory and are taken without temperature control on memory. NVIDIA does not provide guidelines for memory power. For absolute ratings, please contact the memory manufacturer.

SP-09948-001_v07

Table 11. Output EDP-c Specifications

	TGP	NVVDD	FB TOTAL	0.95V Total[1]	1.8V Total[2]
	(W)	(A)	(A)	(A)	(A)
GN20-E5	115	123	38.5	2.1	2.9
	125	124	38.5	2.1	2.9
	135	124	38.5	2.1	2.9
	145	124	38.5	2.1	2.9
	150	124	38.5	2.1	2.9
GN20-E5 Max-Q	80	96	25.6	2.0	2.4
	90	99	25.6	2.0	2.4

	TGP	NVVDD	FB TOTAL	0.95V Total[1]	1.8V Total[2]
	(W)	(A)	(A)	(A)	(A)
GN20-E3	115	123	16.0	2.1	2.9
	125	123	16.1	2.1	2.9
GN20-E3 Max-Q	80	95	28.5	2.0	2.4
	90	99	28.5	2.1	2.4
GN20-E1-KA/-KB/-KC/-KD	80	98	22.8	2.1	2.4
	90	99	22.8	2.1	2.4
	115	99	22.8	2.1	2.9
GN20-E1-Q-KD Max-Q	60	68	22.8	2.1	2.4
	70	74	22.8	2.1	2.4

Notes:
[1] 0.95V Total includes the PCIe and other 0.95V rails except the IFP_IOVDD rail. Add 305 mA for each IFP in use for DP/HDMI.
[2] 1.8V Total includes all PLL, PCIe, 1V8, and other 1.8V rails except the IFPx_PLLVDD power rail. Add 330 mA for each IFP in use.
[3] Power supply rail voltages set to maximum DC tolerance. Worst case current is observed at GPU maximum operating temperature.
[4] FB TOTAL EDPc current is the total of FBVDD+FBVDDQ, which includes GPU and memory EDPc current. These values are with nominal memory and are taken without temperature control on memory. NVIDIA does not provide guidelines for memory power. For absolute ratings, please contact the memory manufacturer.

SP-09936-001_v06

GPU SKU INFORMATION

GN20-E7/-E5/-E4/-E3/-P1/-P0 Summary

GPU	Package	TGP with cTGP (W)	Dynamic Boost (W)	TGP+cTGP +Dynamic Boost (W)	NVVDD	FBVDD
					Regulator	Regulator
GN20-E7	GB5-256	115-150	15	115-165	6-ph/5-ph	2-ph
GN20-E7 MAX-Q	GB5-256	80-90	20	80-110	4-ph	2-ph
GN20-E5/-E4	GB5-256	115-125	15	115-140	5-ph	2-ph
GN20-E5/-E4 MAX-Q	GB5-256	80-90	20	80-110	4-ph	2-ph
GN20-E3	GB5-256	115	15	115-130	5-ph	1-ph
GN20-E3 MAX-Q	GB5-256	60-90	20	60-110	4-ph/3-ph	1-ph
GN20-P1/P0	GB5B-128	60-80	15	60-95	4-ph/3-ph	1-ph
GN20-P1/P0 MAX-Q	GB5B-128	35-50	15	35-65	3-ph/2-ph	1-ph
N18P-G61-A	GB5-128	50-70	15	50-85	3-ph/2-ph	1-ph
N18P-G61-A MAX-Q	GB5-128	35-45	15	35-60	3-ph/2-ph	1-ph

GN20_QN20_GPU_HW_WorkShop_PP-10052-001_v01

GPU SKU INFORMATION

QN20-E5/-E3/-E1/-P3/-P1 Summary

GPU	Package	Standard TGP with cTGP (W)	Dynamic Boost (W)	TGP+cTGP +Dynamic Boost (W)	NVVDD	FBVDD
					Regulator	Regulator
QN20-E5	GB5-256	115-150	15	115-165	6-ph/5-ph	2-ph
QN20-E5 Max-Q	GB5-256	80-90	20	80-110	4-ph	2-ph
QN20-E3	GB5-256	115-125	15	115-140	5-ph	2-ph
QN20-E3 Max-Q	GB5-256	80-90	20	80-110	4-ph	2-ph
QN20-E1	GB5-256	115	15	115-130	5-ph	1-ph
QN20-E1 Max-Q	GB5-256	60-90	20	60-110	4-ph/3-ph	1-ph
QN20-P3	GB5B-128	60-80	15	60-95	4-ph/3-ph	1-ph
QN20-P3 Max-Q	GB5B-128	35-50	15	35-65	3-ph/2-ph	1-ph
QN20-P1	GB5-128	60-80	15	60-95	3-ph/2-ph	1-ph
QN20-P1 Max-Q	GB5-128	35-50	15	35-65	3-ph/2-ph	1-ph

Note: Using cTGP Mode 2, Max-Q GPU can go up to Standard TGP

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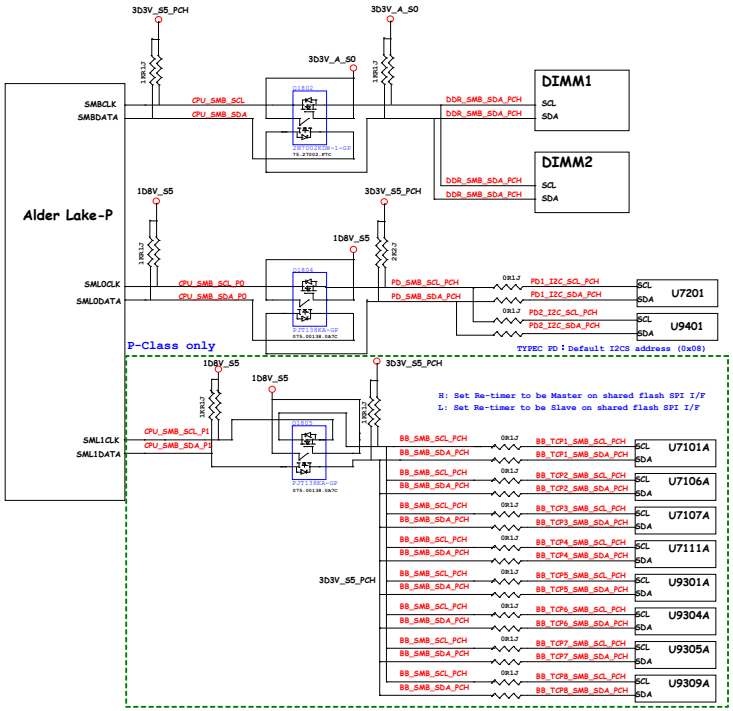
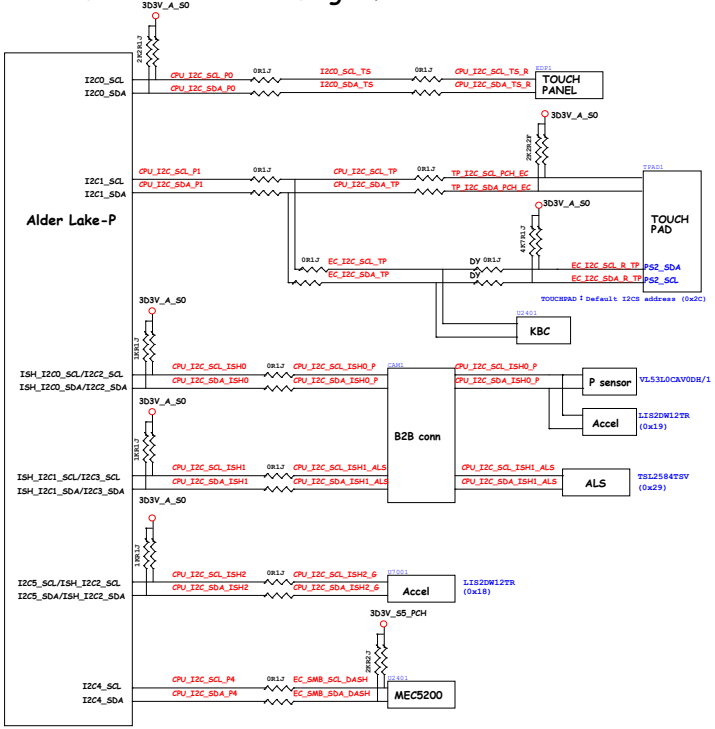
Alder Lake-P SMBus/SMLink Block Diagram



Alder Lake-P I2C Block Diagram



KBC SMBus Block Diagram

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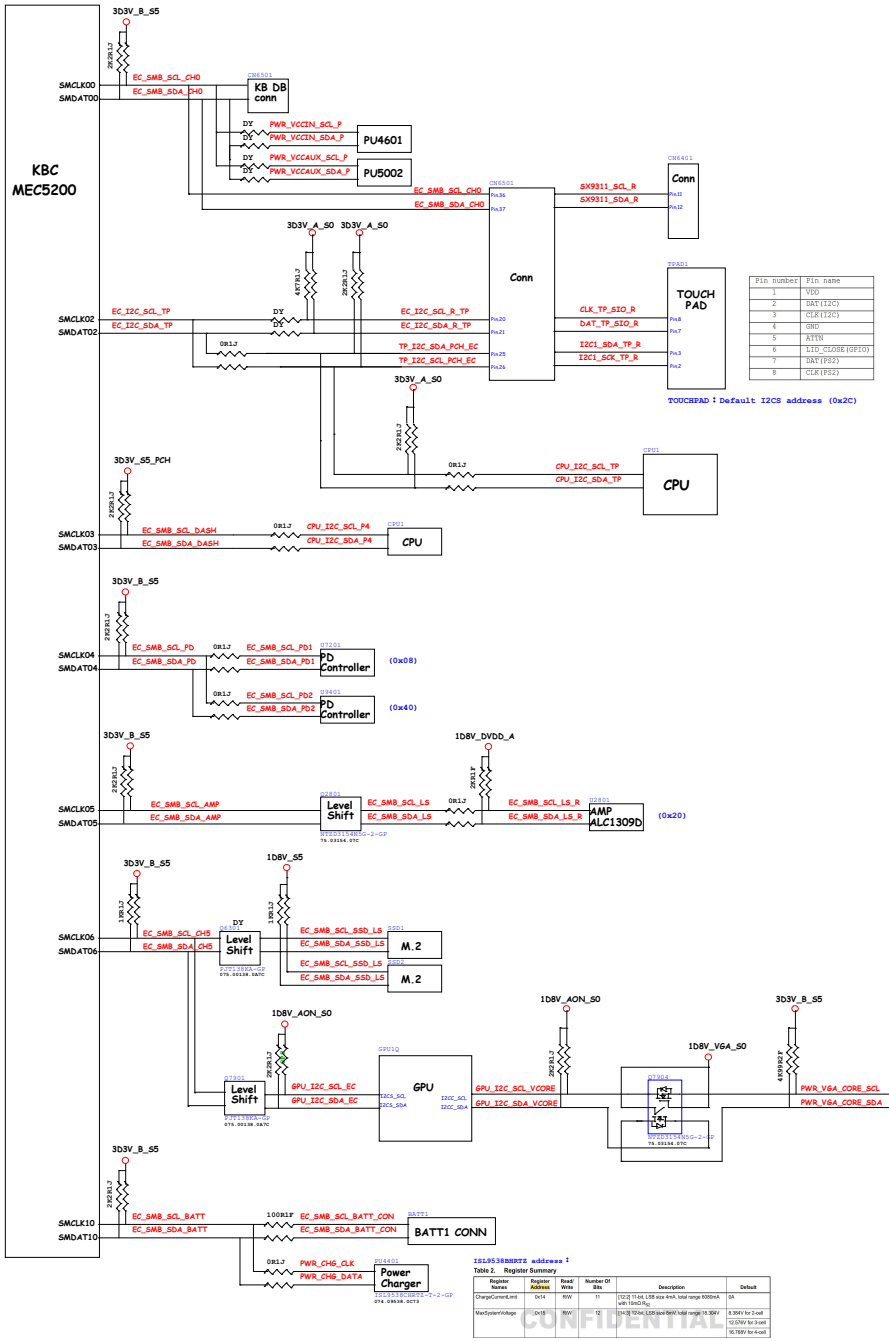

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	LID_CLOSE(GPIO)
7	DAT(PS2)
8	CLK(PS2)

ISL9538HRTZ address :

Table 2. Register Summary

Register Names	Register Address	Read/ Write	Number Of Bits	Description	Default
ChargeCurrentLimit	0x14	R/W	11	[12:2] 11-bit, LSB size 4mA, total range 8000mA with 10mΩ R_{SNS}	0A
MaxSystemVoltage	0x15	R/W	12	[14:3] 12-bit, LSB size 8mV, total range 16.304V	8.304V for 2-cell 12.576V for 3-cell 16.768V for 4-cell

MP2884AGU address :

PMBus Address	Setting Point(V)	R_{ADDR0} (kΩ) 1%	R_{ADDR1} (kΩ) 1%
20h	0	3.32	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	6.66
2Fh	1.500	3.32	16.5

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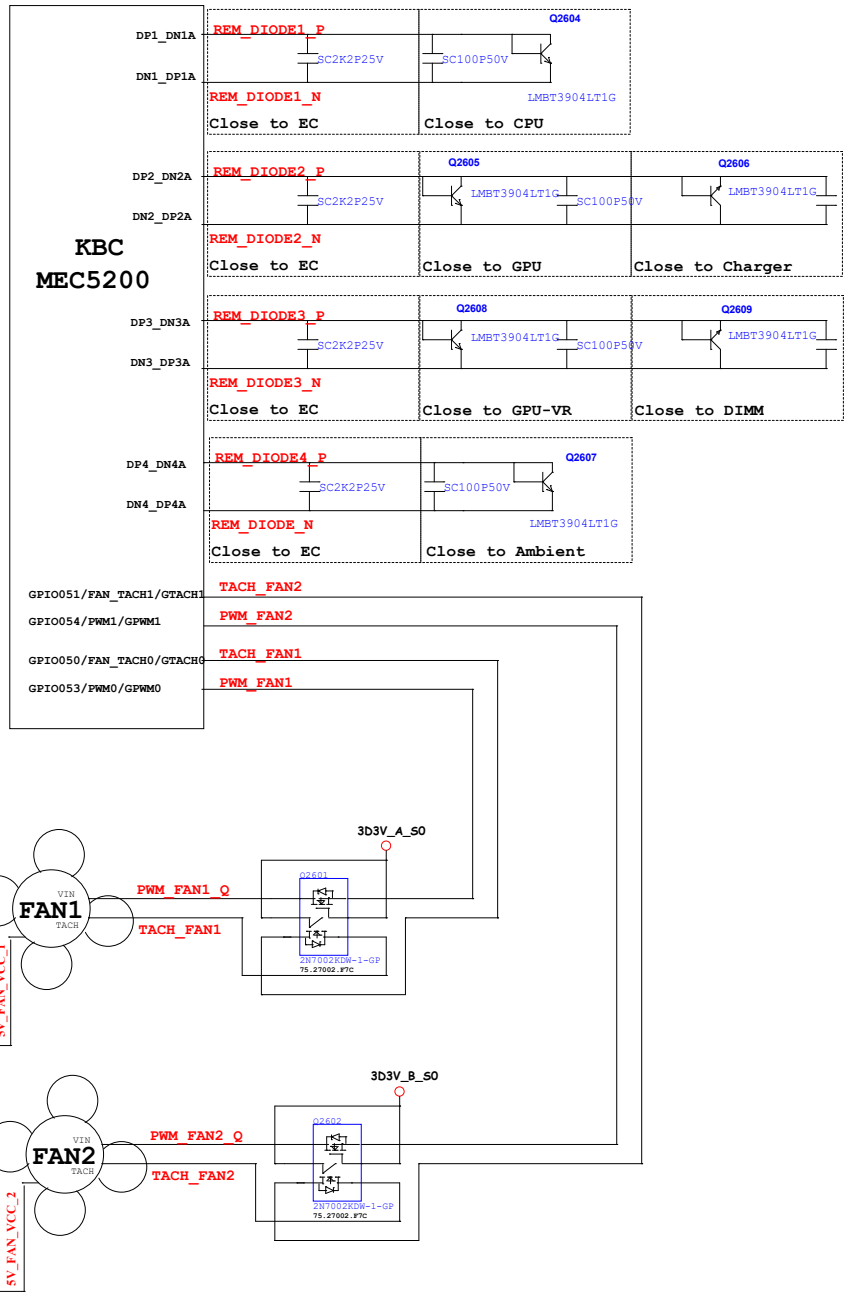
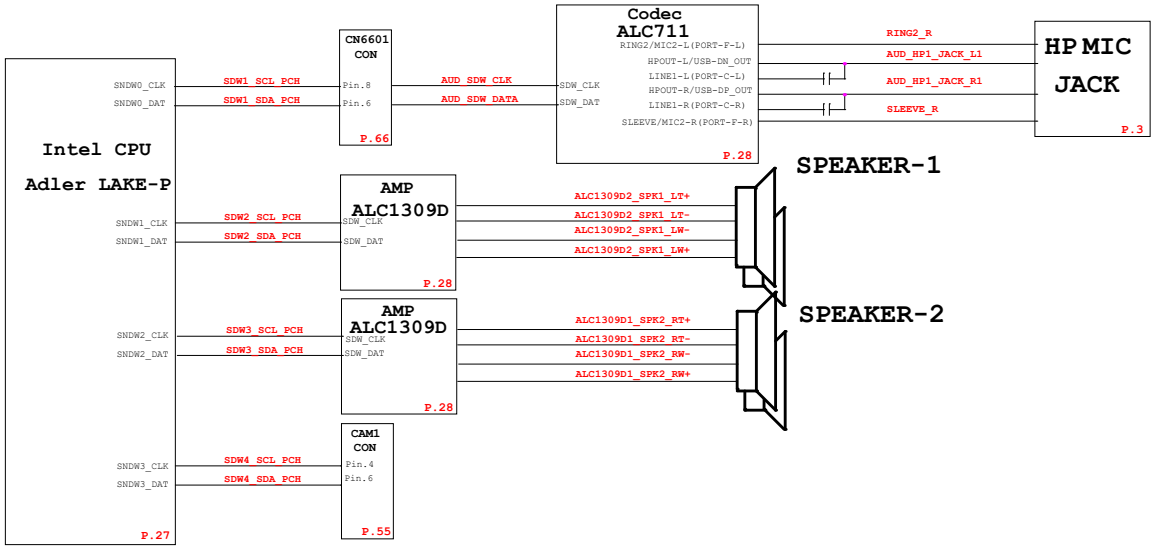
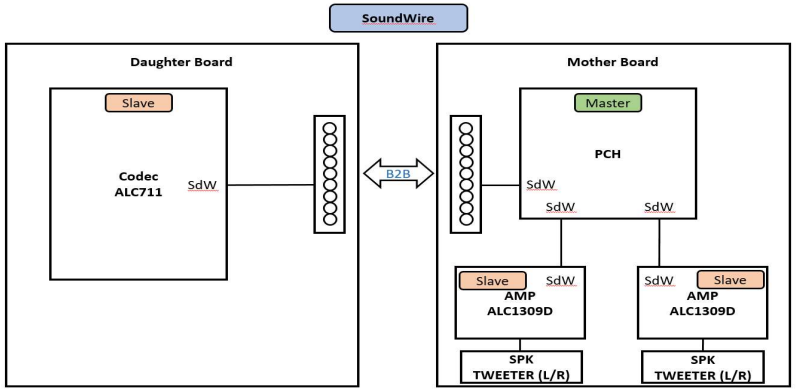
Thermal Block Diagram



Audio Block Diagram





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CLK Block Diagram

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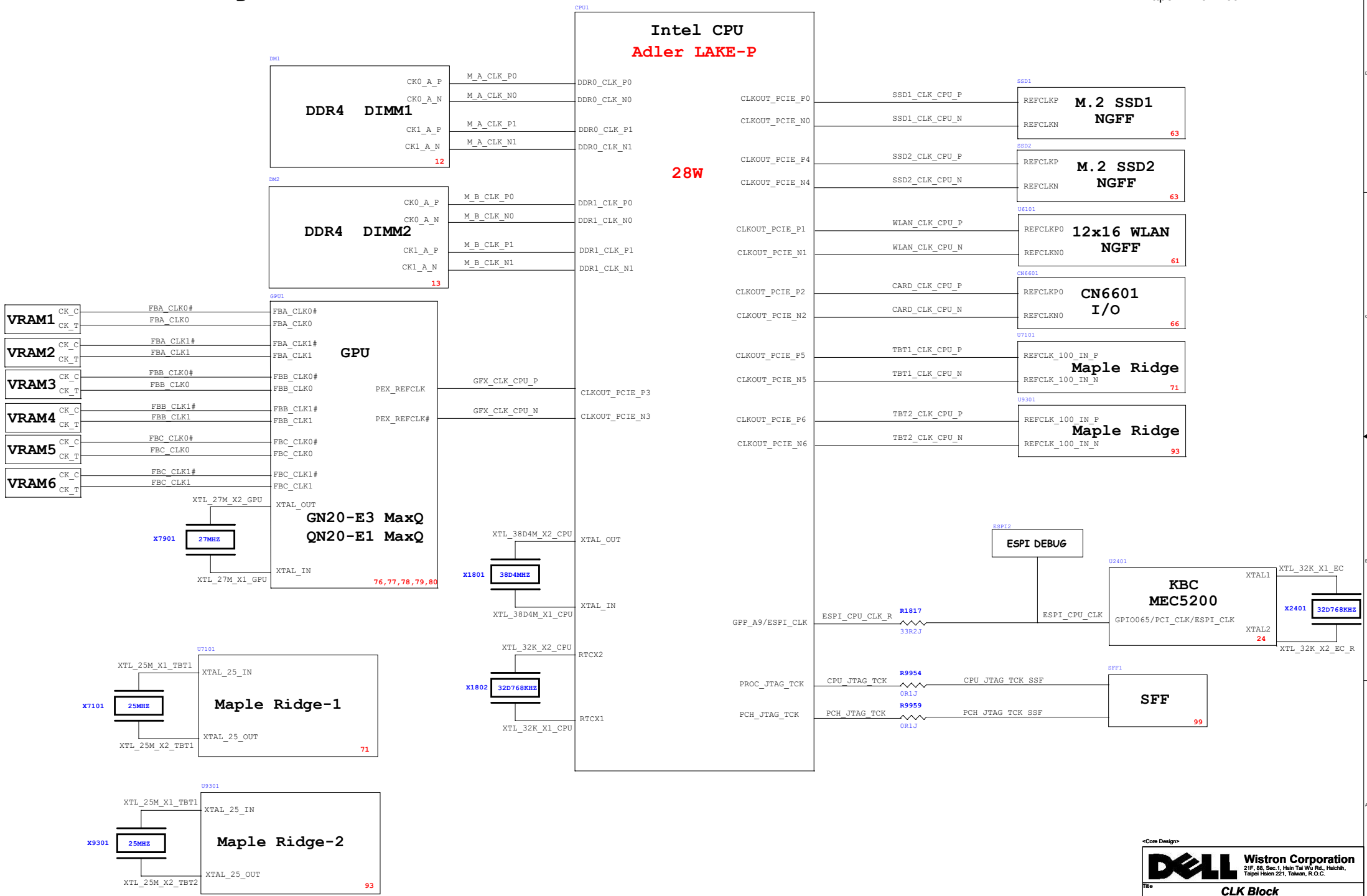

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Title: CLK Block

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